DVD RECORDER

DRX-1

SERVICE MANUAL

IMPORTANT NOTICE

This manual has been provided for the use of authorized YAMAHA Retailers and their service personnel.
It has been assumed that basic service procedures inherent to the industry, and more specifically YAMAHA Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components, and failure of the product to perform as specified. For these reasons, we advise all YAMAHA product owners that any service required should be performed by an authorized YAMAHA Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification or recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of YAMAHA are continually striving to improve YAMAHA products. Modifications are, therefore, inevitable and specifications are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and part replacement. Recheck all work before you apply power to the unit.

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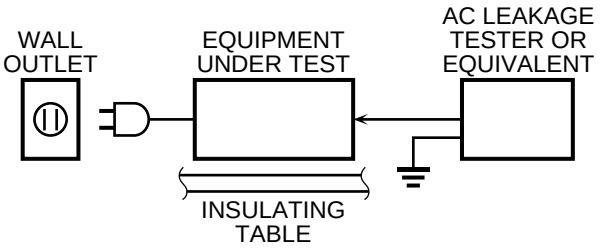
100821

YAMAHA
YAMAHA CORPORATION
P.O.Box 1, Hamamatsu, Japan

■ TO SERVICE PERSONNEL

1. Critical Components Information
   Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.
2. Leakage Current Measurement (For 120V Models Only)
   When service has been completed, it is imperative to verify that all exposed conductive surfaces are properly insulated from supply circuits.

- Meter impedance should be equivalent to 1500 ohm shunted by 0.15μF.



- Leakage current must not exceed 0.5mA.
- Be sure to test for leakage with the AC plug in both polarities.

THE DVD AUDIO/VIDEO RECEIVER SHOULD NOT BE ADJUSTED OR REPAIRED BY ANYONE EXCEPT PROPERLY QUALIFIED SERVICE PERSONNEL.

CAUTION
1120: FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE 2.5A, 250V FUSE.

CAUTION
1120: REPLACE WITH SAME TYPE 2.5A, 250V FUSE.

ATTENTION
1120: UTILISER UN FUSIBLE DE RECHANGE DE MEME TYPE DE 2.5A, 250V.

WARNING: CHEMICAL CONTENT NOTICE!

The solder used in the production of this product contains LEAD. In addition, other electrical/electronic and /or plastic (where applicable) components may also contain traces of chemicals found by the California Health and Welfare Agency (and possibly other entities) to cause cancer and/or birth defects or other reproductive harm.

DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHATSOEVER!

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

WARNING: Laser Safety

This product contains a laser beam component. This component may emit invisible, as well as visible radiation, which may cause eye damage. To protect your eyes and skin from laser radiation, the following precautions must be used during servicing of the unit.

1) When testing and/or repairing any component within the product, keep your eyes and skin more than 30 cm away from the laser pick-up unit at all times. Do not stare at the laser beam at any time.

2) Do not attempt to readjust, disassemble or repair the laser pick-up, unless noted elsewhere in this manual.

3) CAUTION: Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Laser Emitting conditions:

1) When the Top Cover is removed and the "STANDBY/ON" SW is turned to the "ON" position, the laser component will emit a beam for several seconds to detect if a disc is present. During this time (5 - 10 sec.) the laser may radiate through the lens of the laser pick-up unit. Do not attempt any servicing during this period!
   If no disc is detected, the laser will stop emitting the beam. When a disc is loaded, you will not be exposed to any laser emissions.

2) The laser power level can be adjusted with the VR on the pick-up PWB. However, this level has been set by the factory prior to shipping from the factory. Do not adjust this laser level control unless instruction is provided elsewhere in this manual. Adjustment of this control can increase the laser emission level from the device.

Laser Diode Properties

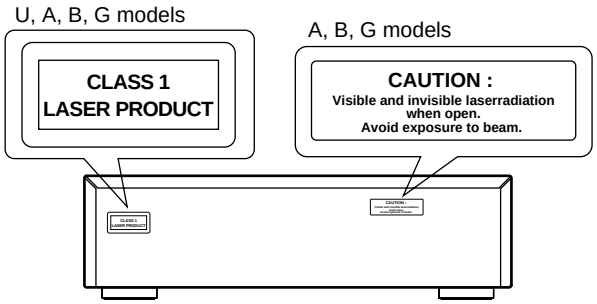
Type:	InGaAIP Semiconductor laser (DVD)
	AlGaAs Semiconductor laser (CD)
Wave length:	660 nm (DVD)
	780 nm (VCD/CD)
Output Power:	20 mW (DVD writing)
(out of objective)	0.8 mW (DVD reading)
	0.3mW (CD reading)
Beam divergence:	82 degree (DVD)
	54 degree (CD)

VARO! : AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄkymÄTTÖMÄLLE LASER-SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

VARNING! : OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player



WARNING LOCATION: REAR PANEL

CAUTION VISIBLE AND INVISIBLE LASER RADIATION.WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO!AVATTAESSA OLET ALTTIINA NÄKYV¨ALLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION.WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Warning for power supply

The primary side of the power supply carries live mains voltage when the player is connected to the mains even when the player is switched off !
This primary area is not shielded so it is possible to touch copper tracks and/or components when servicing the player. Service personnel have to take precautions to prevent touching this area or components in this area .
The primary side of the power supply has been indicated with a lightening stroke and a stripe-marked print on the printed wiring board

Note:
The screws on the DVDR mechanism (position 1 in on the exploded view drawing) may never be touched, removed or re-adjusted.
Handle the DVDR mechanism with care when the unit has to be exchanged!
The DVDR mechanism is very sensitive for dropping or giving shocks.

■ PREVENTION OF ELECTRO STATIC DISCHARGE

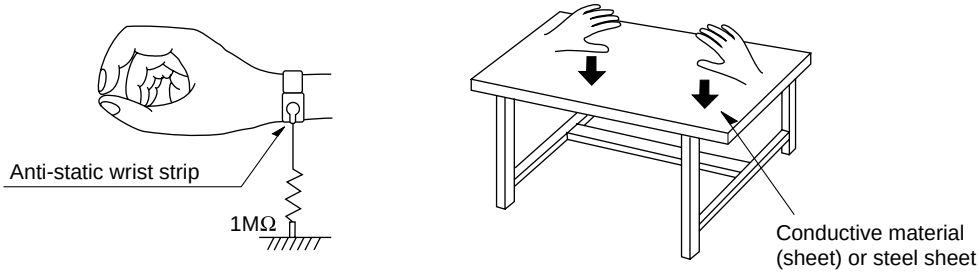
The laser diode in the DVDR mechanism may be damaged due to static electricity from clothes or the human body. Use caution to prevent electrostatic damage when servicing or handling the DVDR mechanism.

1. Grounding for electrostatic damage prevention

Some devices, such as the DVD recorder, use an optical pickup (laser diode) that will be damaged by static electricity in the working environment. Only attempt service after ensuring that all grounding procedures have been completed.

1. Worktable grounding
   Put a grounded conductive material (sheet) or iron sheet on the area where the optical pickup is placed.

2. Human body grounding
   Use an anti-static wrist strap to discharge the static electricity from your body.



2. Handling Precautions for DVDR mechanism

1. Handle the DVDR mechanism gently, as it is an extremely high-precision assembly.
2. The flexible cable lines may break if an excessive force is applied to it. Use caution when handling the cable.
3. The semi-fixed resistor for laser power adjustment should not be adjusted. Do not turn the resistor.

■ LOCALE MANAGEMENT INFORMATION

Locale Management Information : This DVD recorder is designed and manufactured to respond to the Locale Management Information that is recorded on the DVDR disc. If the Locale number described on the DVDR disc does not correspond to the Locale number of this DVD recorder, this DVD recorder cannot play this disc.

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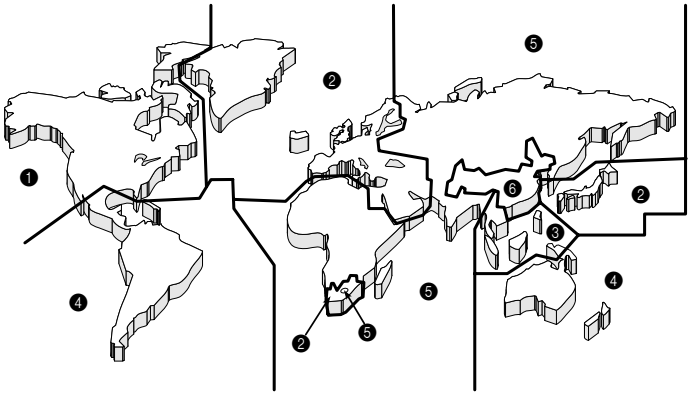
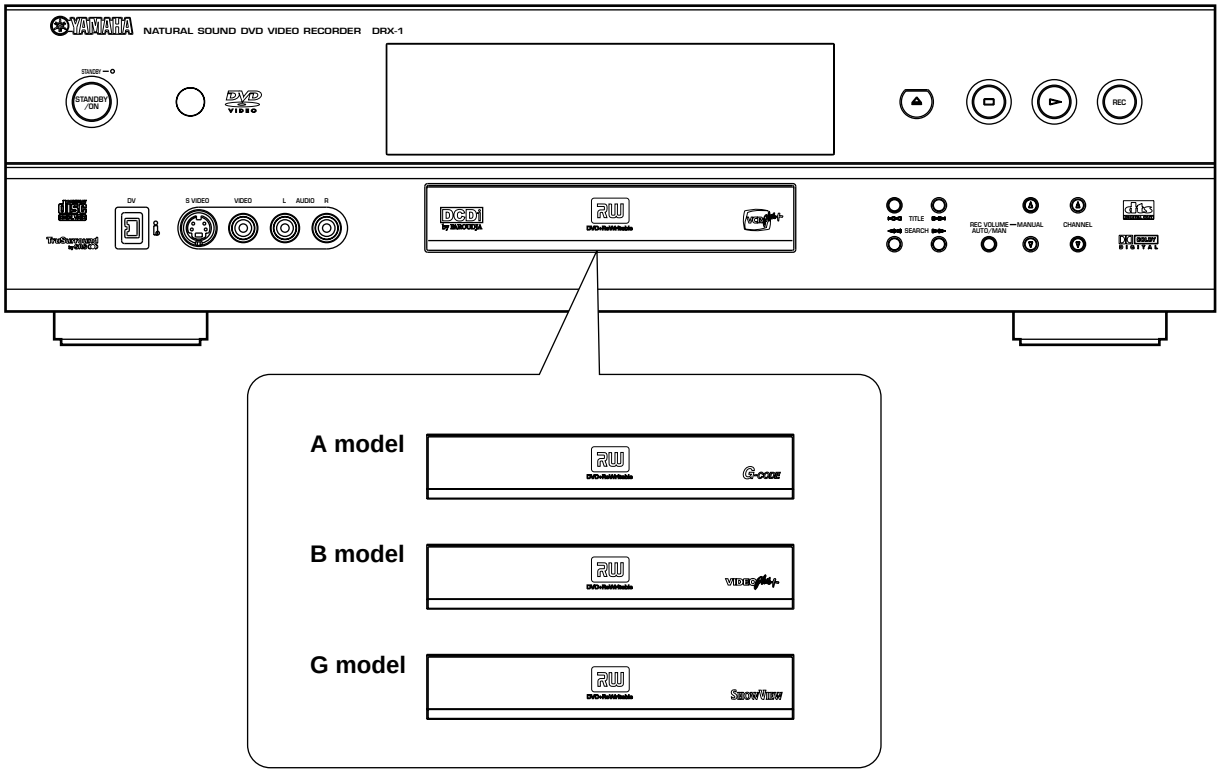
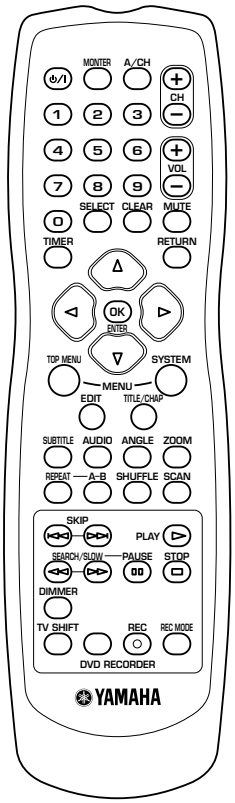


■ FRONT PANELS

U model

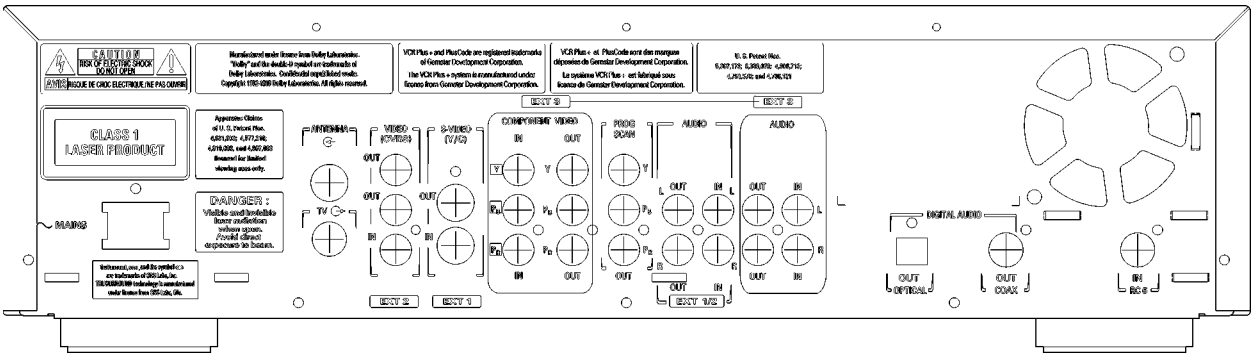


■ REMOTE CONTROL

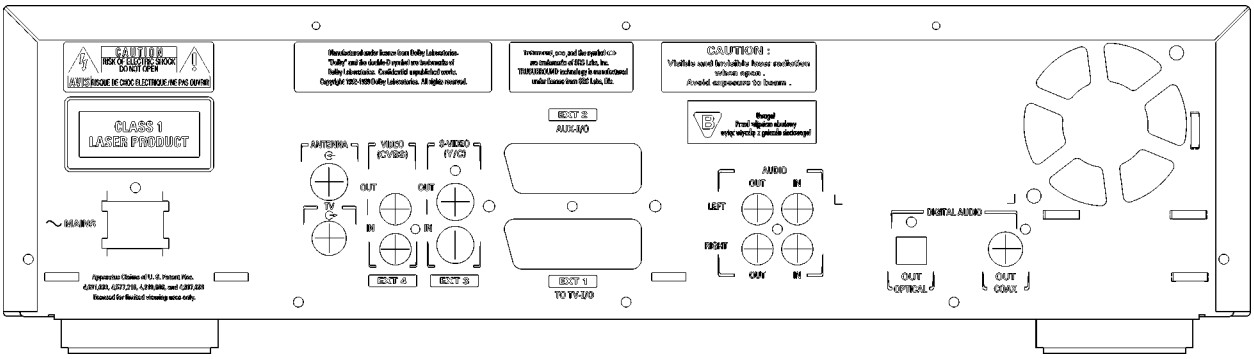


■ REAR PANELS

U model



A, B, G models



■ SPECIFICATIONS

DISC FORMATS SUPPORTED

Disc type	Playback	Recording
DVD+RW	•	•
DVD+R	•	•
DVD-RW (Video format)	•	—
DVD-R	•	—
DVD-Video	•	—
SVCD	•	—
Video CD	•	—
Audio CD	•	—
CD-R	•	—
CD-RW	•	—

RECORDABLE DISC FORMATS

Medium	DVD+RW: Phase-Change ReWritable DVD+R: dye-based
Diameter	12 cm
Capacity (single side)	4.7 Gbyte
Recording time	HQ 60’ 9.72 Mbit/s SP+ 150’ 4.06 Mbit/s EP 240’ 2.54 Mbit/s EP+ 360’ 1.69 Mbit/s

	A, B, G models	U model
TV Standard	PAL/SECAM	NTSC
Scan Frequency	50Hz	60Hz
Number of lines	625	525
Playback	•	•
Recording	•	•
Internal tuner	•	•

VIDEO FORMAT

Digital Compression	MPEG2 for DVD MPEG1 for VCD

VIDEO RESOLUTION 50Hz 60Hz

DVD-Video/ DVD+RW(HQ/SP+)		
• Horiz. Resolution	720 pixels1	720 pixels1
• Vertical Resolution	576 lines	480 lines
DVD+RW (EP/EP+)		
• Horiz. Resolution	360 pixels2	360 pixels2
• Vertical Resolution	576 lines	480 lines
VCD		
• Horiz. Resolution	352 pixels	352 pixels
• Vertical Resolution	288 lines	240 lines

1 equivalent to 500 lines on your TV
2 equivalent to 250 lines on your TV

VIDEO PERFORMANCE

DA Converter	10-bit
AD Converter	9-bit
Signal handling	Components
Video Output	1 Vpp into 75 Ohm
S-video Output	Y: 1 Vpp into 75 Ohm C: 0.300 Vpp into 75 Ohm
Component/Progressive out	Y: 1Vpp into 75 Ohm (U model) Pb: 0.7 Vpp into 75 Ohm (U model) Pr: 0.7 Vpp into 75 Ohm (U model)
RGB Output	0.7 Vpp into 75 Ohm (A, B, G models)

AUDIO FORMAT

Compressed digital	Playback	Recording
• Dolby Digital (AC-3)	Multi-channel	2-channel 16 bit, fs 48 kHz
• DTS	Multi-channel	—
• MPEG1	2-channel	—
Uncompressed digital (SPDIF)		
• PCM	2-channel 16, 20, 24 bit fs 48 kHz	—

AUDIO PERFORMANCE

DA Converter	24 bit	
AD Converter	16 bit	
DVD	fs 96 kHz	4 Hz - 44 kHz
	fs 48 kHz	4 Hz - 22 kHz
Video CD	fs 44.1 kHz	4 Hz - 20 kHz
Audio CD	fs 44.1 kHz	4 Hz - 20 kHz
Signal-Noise (1kHz)	105 dB	
Dynamic Range (1kHz)	100 dB	
Crosstalk (1kHz)	110 dB	
Distortion/Noise (1kHz)	90 dB	

PROGRAMMING

Number of events	6; 1 year; Daily/Weekly
Programming mode	OTR, Remote
Timer programming	
Manual, the VCR Plus+ system (U model)	
Manual, VIDEO Plus+, NexTView Link (B model)	
Manual, SHOWVIEW, NexTView Link (G model)	
Manual, G-CODE, NexTView Link (A model)	
Record Control and transmitter identification	PDC, VPS (B, G models)

DISC RECORDING

- One-Touch Recording (OTR)
- Safe Recording
- Direct Recording (A, B, G models)
- Append
- Divide
- Erase
- Automatic/Manual Chapter Marker insertion
- Disc write lock
- Index Picture Screen
- Custom Index Pictures
- Automatic/Manual Audio Recording Level

DISC PLAYBACK

- Auto Resume (20 disc)
- Play / Stop / Pause
- Fast Forward/Backward (three speeds)
- Step Forward/Backward
- Slow (three speeds)
- Title / Track Select
- Next / Previous Title / Track / Chapter
- Repeat (Chapter / Title / All) or (Track / All)
- A-B Repeat
- Intro Scan
- Perfect Still with digital multi-tap filter
- Zoom (x1.33, x2, x4) with picture enhancement
- Pan

GENERAL FUNCTIONALITY

- 3D sound (SRS TruSurround)
- Beep Feedback for Remote Control
- Backup Presets & Timer Events: 1 year
- Backup Clock & Calendar: 7 hours
- Time & Date Download

POWER SUPPLY

Power supply	
U model	100 - 120V, 60Hz
A, B, G models	220 - 240V, 50/60 Hz
Power consumption Operation	
U model	36 W
A, B, G models	33 W
	Low-power standby 3 W

CABINET

Dimensions (WxHxD)	435 x 120 x 330 (17 x 4.8 x 13 inches)
Net Weight	13.9 lb. (6.3 kg)
Front Panel	3mm Aluminum

ACCESSORIES

- Remote Control with separately-packed batteries
- 2-core power cord
- Component video cable (U nodel)
- SCART cable (A, B, G models)
- S-Video cable
- Antenna cable
- Audio cable (x 2: U model / x 1: A, B, G models)
- Video cable
- DVD+RW disc

If any item is damaged or missing, please inform your supplier without delay.
Keep the packaging materials; you may need them to transport your Recorder in the future.

* Specifications are subject to change without notice due to product improvements.

U ..... U.S.A. model
B ..... British model
G ..... Europe model
A ..... Australia model

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See exploded view for item numbers

Cover 151
⇒ Remove 9 screws
171 → 174 at both sides
175 → 179 at the rearside
⇒ Lift the cover at the rearside tp remove

mounting ↑ ↓ demounting

Front assy
⇒ open the tray and remove the tray front 65
⇒ remove 4 screws 75 → 78 (front assy → frame 181)
⇒ unlock the front from the frame by releasing successively 6 snaps. (1 on the left, 2 in the middle, 1 on the reight and 2 in the bottom of the frame. The snaps in the bottom can be released inside the set via the holes in the bottom.)

Analog board 1003
⇒ remove the connections
⇒ remove 1 screw (215) (board → frame)
⇒ remove screws 271 → 279 (cinches → backplate)
⇒ remove nut 269 (tuner → backplate)
⇒ release the snaps of 4 spacers 185 → 188 (board → frame)
⇒ demount the board

DVIO board 1005 (DVDR985)
⇒ Remove 2 scrws 217 and 218 (DVIO board → frame 181)
⇒ Release the snaps of 2 spacers (DVIO board → Digital board)
⇒ demount carefully the board. (board to board connection to the Digital board)

Digital board 1001
⇒ Remove the connections
⇒ Remove 4 scrws 207 → 210 (Digital board → frame 181)
⇒ demount the board.

DVDR LOADER 81
⇒ Remove the connections
⇒ Remove 4 screws (192 → 195) (air filter 196 → loader 81)
⇒ Remove screw 196 (air filter inlet 191 → frame 181)
⇒ Remove air filter assy
⇒ Open the tray and remove the tray front 65
⇒ Remove 4 screws 200 → 203 (loader 81 → frame 181)
⇒ Demount the DVDR loader

Switched Operating Power supply 1002
⇒ Remove the connections
⇒ Remove screws 204 → 206 (board → frame)
⇒ Remove screw 268 (mains inlet → backplate)
⇒ Release the snaps of 2 spacers 186 and 184 (board → frame)
⇒ Demount the board

FRONT DV Board 1006 (DVDR985)
⇒ Remove scrw 17 (board → front)
⇒ demount the board

Display board 1001
⇒ Remove 8 screws 31 → 38 (board → front)
⇒ demount the board

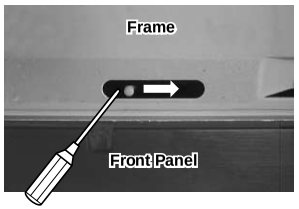
IR/STBY Board 1001
⇒ remove screws 41+42 (board → front)
⇒ demount the board

FRONT AV Board 1007
⇒ remove screws 48+49 (board → front)
⇒ demount the board

Manually removal of tray front 65

In case the loader is defective and cannot be opened electrically, you can open the tray as follows:

⇒ Via a hole in the frame and by way of a screwdriver, it is possible tp unlock the tray. Push the white pin of the slider at the bottom side of the loader to the left.
⇒ Open the unlocked tray.

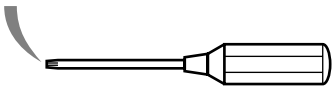


When disassembling, use the special screw driver with tip shape in figure.

T10 2.7 mm for screws 21, 34 and 35

T8 2.2 mm for screws 32

T6 1.7 mm for screws 22, 31 and 33



■ SERVICE POSITION

● Front

Front

Photo 1

● DVIO board

To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

DVIO Extender

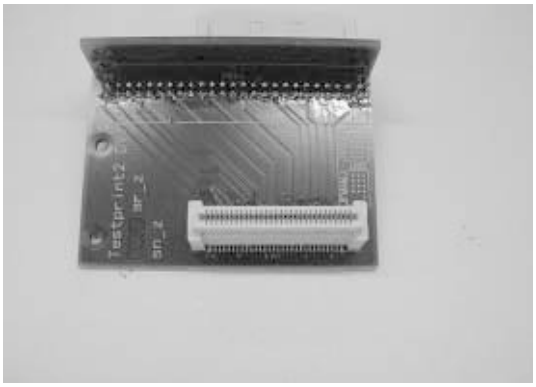


Photo 2

DVIO 1

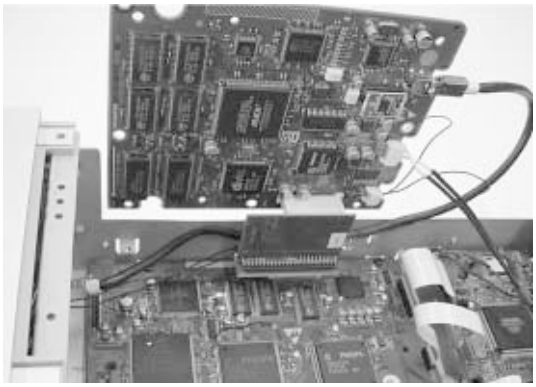


Photo 3

DVIO 2

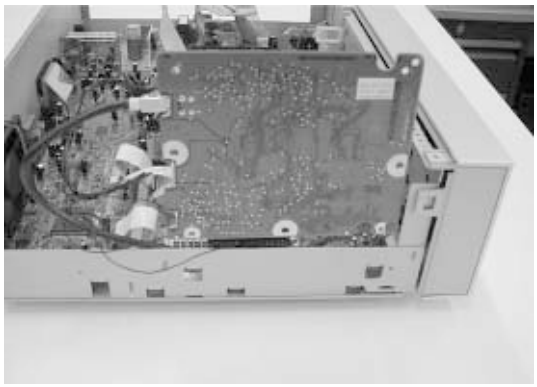


Photo 4

● Digital board

After demounting of DVIO board, the top side of the digital board is in reach. To reach the bottom side of the digital board, the DVDR module must be demounted together with the digital board. Connected to each other, the assembly can be set in a service position. In this position, the bottom side of the digital board and the servo board are in reach to be serviced.

Digital 1

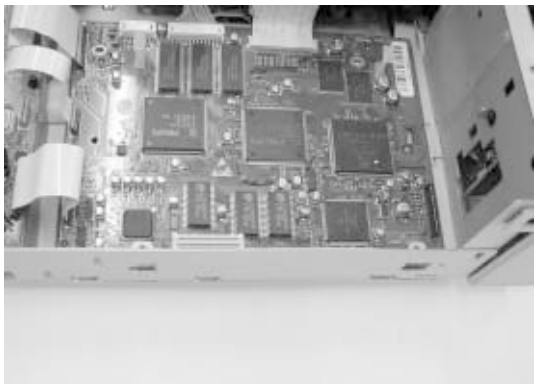


Photo 5

Digital 2

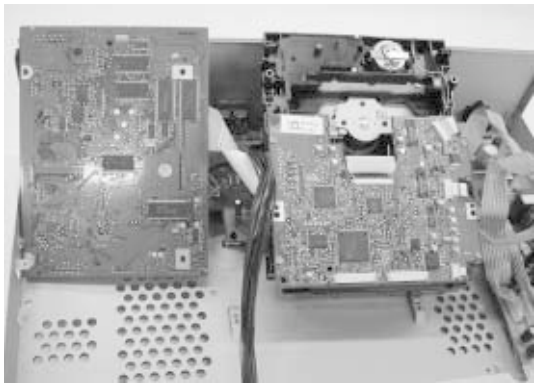


Photo 6

● Analog board

To put the analog board in service position, demount the assembly of analog board and backplate as follows:

1. Remove 3 screws from the backplate to the frame
2. Remove the screw from the backplate to the mains inlet of the power supply
3. Remove the screw of the analog board to the frame
4. Release the snaps of the 4 spacers of the analog board to the frame.
   Turn the assembly of the backplate and the analog board against the loader.

Analog (A, B, G models)

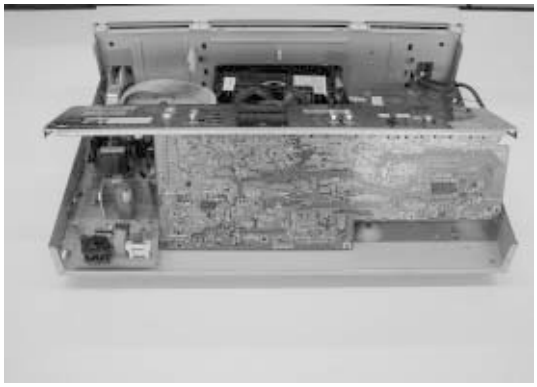


Photo 7

Analog (U model)

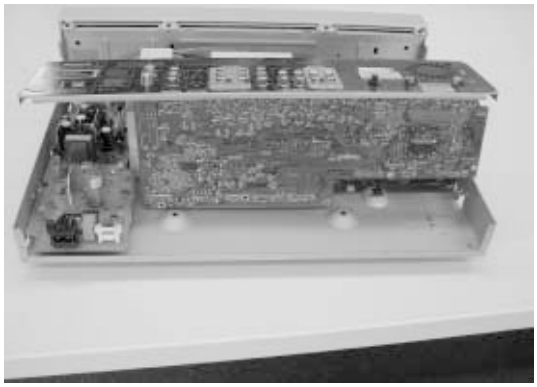


Photo 8

■ DIAGNOSTIC SOFTWARE

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

1. End user/Dealer script interface
2. Player script interface
3. Menu and command interface

1. End User/Dealer Script Interface

1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder; no other equipment is needed. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

1.2 Contents

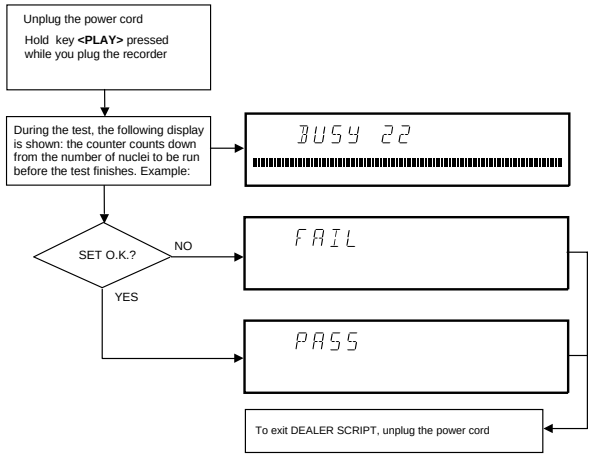

Unplug the power cord
Hold key <PLAY> pressed while you plug the recorder
During the test, the following display is shown: the counter counts down from the number of nuclei to be run before the test finishes. Example:
BUSY 22
SET O.K.?
NO
YES
FAIL
PASS
To exit DEALER SCRIPT, unplug the power cord

Fig. 1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder. The nuclei called in the End user/Dealer script are the following:

Counter	Nucleus	Name	Description
22	104	HostdSdramWrR	checks all memory locations of the 4MB SDRAM
21	106	HostdDramWrR	checks all the DRAM connected to the microprocessor of the digital board
20	123	HostdI2cNvram	checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM
19	202	SAA7118I2c	checks the interface between the Host I2C controller and the AVENC SAA7118 Video Input Processor
18	200	VideoEncI2c	checks the interface between the host I2C controller and Empress SAA6752
17	207	AudioEncI2c	checks the I2C connection between the host decoder and Empress SAA6752
16	204	AudioEncAccess	tests the HIO8 interface lines between the host decoder and the audio encoder
15	203	AudioEncSramAccess	checks the access of the SRAM by the audio encoder (address and data lines).
14	205	AudioEncSramWrR	tests the SRAM connected to the audio encoder
13	206	AudioEncInterrupt	tests the interrupt line between the host decoder and the audio encoder
12	300	VsmAccess	checks whether the VSM interrupt controllers and DRAM are accessible
11	303	VsmInterrupt	checks both interrupt lines between the VSM and the host decoder
10	302	VsmSdramWrR	tests the entire SDRAM of the VSM
9	1400	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	1401	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	601	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	500	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	700	AnalogueEcho	checks the interface between the host processor and the microprocessor on the analogue board
4	711	AnalogueNvram	checks the NVRAM on the analogue board

3	706	AnalogueTuner	checks whether the tuner on the analogue board is accessible
2	901	LoopAudioUserDealer	This nucleus tests the components on the audio signal path The host decoder - The analogue board - The audio encoder - The VSM On the analogue board the audio is internally looped back to the digital board
1	906	LoopVideoUserDealer	Nucleus for testing the components on the video signal system path: - The VIP - The video encoder - The VSM - The host decoder - The analogue board On the analogue the video signal is internally routed back to the digital board.•5.2 Player Script Interface

2. Player Script Interface

2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD recorder's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.

To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the DVDR module) require that a DVD+RW disc is inserted.

Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

2.2 Structure of the Player Script

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module.

Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

- Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP	DESCRIPTION	NUCLEUS
1	Press OPEN/CLOSE and PLAY at the same time and POWER ON the recorder to start the playerscript	2
2	The local display shows FPSEGMENTS. Press PLAY to start the test. First the starburst pattern is lit, then the horizontal segments are lit, followed by the vertical segments and the last test is light all segments test. After each of the 4 tests the user has to confirm that the correct pattern was lit. Press PLAY to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press RECORD to indicate that the correct pattern was not successfully lit. Press STOP to skip this nucleus.	502
3	The local display shows FPLABELS. Press PLAY to start the test. Press PLAY to confirm that all labels are lit. Press RECORD to indicate that not all labels are lit. Press STOP to skip this nucleus.	503
4	The local display shows FPLIGHT ALL. Press PLAY to start the test. Press PLAY to confirm that everything was lit. Press RECORD to indicate that not all patterns are lit. Press STOP to skip this nucleus.	520

STEP	DESCRIPTION	NUCLEUS
5	The local display shows FPLED. Press PLAY to start the test. Press PLAY to confirm that the led is lit. Press RECORD to indicate that the led is not lit. Press STOP to skip this nucleus.	504
6	The local display shows FPFLAP OPEN. Press PLAY to start the test. Press PLAY to confirm that the flap has opened. Press RECORD to indicate that the flap did not open. Press STOP to skip this nucleus.	522
7	The local display shows FPKEYBOARD. Press PLAY to start the test. Attention all keys have to be pressed to get a positive result! Press PLAY for more than one second to confirm that all the keys were pressed and shown on the local dis-play. If not all the keys were pressed, a FAIL message will appear on the local display. Press RECORD for more than one second to indicate that not all keys were pressed and shown on the local display. Press STOP for more than one second to skip this nucleus.	505
8	The local display shows FPREMOTE CONTROL. Press PLAY to start the test. Press PLAY to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result. Press RECORD to indicate that the key on the remote control was pressed but not shown on the local display. Press STOP to skip this nucleus.	506
9	The local display shows FPDIMMER. Press PLAY to start the test. Press PLAY to confirm that the text on the local display was dimmed. Press RECORD to indicate that the text on the local display was not dimmed. Press STOP to skip this nucleus.	518
10	The local display shows FPBEEPER. Press PLAY to start the test. Press PLAY to confirm that the beeper on the front panel sounded. Press RECORD to indicate that the beeper on the front panel did not sound. Press STOP to skip this nucleus.	514
11	The local display shows FPFLAP CLOSE. Press PLAY to start the test. Press STOP to skip this nucleus.	523
12	The local display shows ROUTE VIDEO. Press PLAY to start the test. Press STOP to skip this nucleus.	712
13	The local display shows ROUTE AUDIO. Press PLAY to start the test. Press STOP to skip this nucleus.	713
14	The local display shows COLOUR-BAR ON. Press PLAY to start the test. Press STOP to skip this nucleus.	120
15	The local display shows PINK NOISE ON. Press PLAY to start the test. Press STOP to skip this nucleus.	115
16	The local display shows PINK NOISE OFF. Press PLAY to start the test. Press STOP to skip this nucleus.	116
17	The local display shows SINE ON. Press PLAY to start the test. Press STOP to stop the sine. Press STOP to skip this nucleus.	117
18	The local display shows COLOUR-BAR OFF. Press PLAY to start the test. Press STOP to skip this nucleus.	121
19	The local display shows BERESET. Press PLAY to start the test. Press STOP to skip this nucleus.	603
20	The local display shows BETRAY OPEN. Press PLAY to start the test. Press STOP to skip this nucleus.	616
21	The local display shows BETRAY CLOSE. Press PLAY to start the test. Press STOP to skip this nucleus.	615

STEP	DESCRIPTION	NUCLEUS
22	The local display shows BEWRITE READ. Press PLAY to start the test.	617
	Press STOP to skip this nucleus.	
23	The local display shows BETRAY OPEN. Press PLAY to start the test. Press STOP to skip this nucleus.	616
24	The local display shows BETRAY CLOSE. Press PLAY to start the test. Press STOP to skip this nucleus.	615
25	The local display shows READ ERRORLOG. Press PLAY to start the test. Press STOP to skip this nucleus. If the player test succeeded, the user/dealer script will start in an endless loop. If the player test failed, the local display will display FAIL and the error code	633

Remark

In case of failure, the display shows " FAIL XXXXXX ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.

Player script

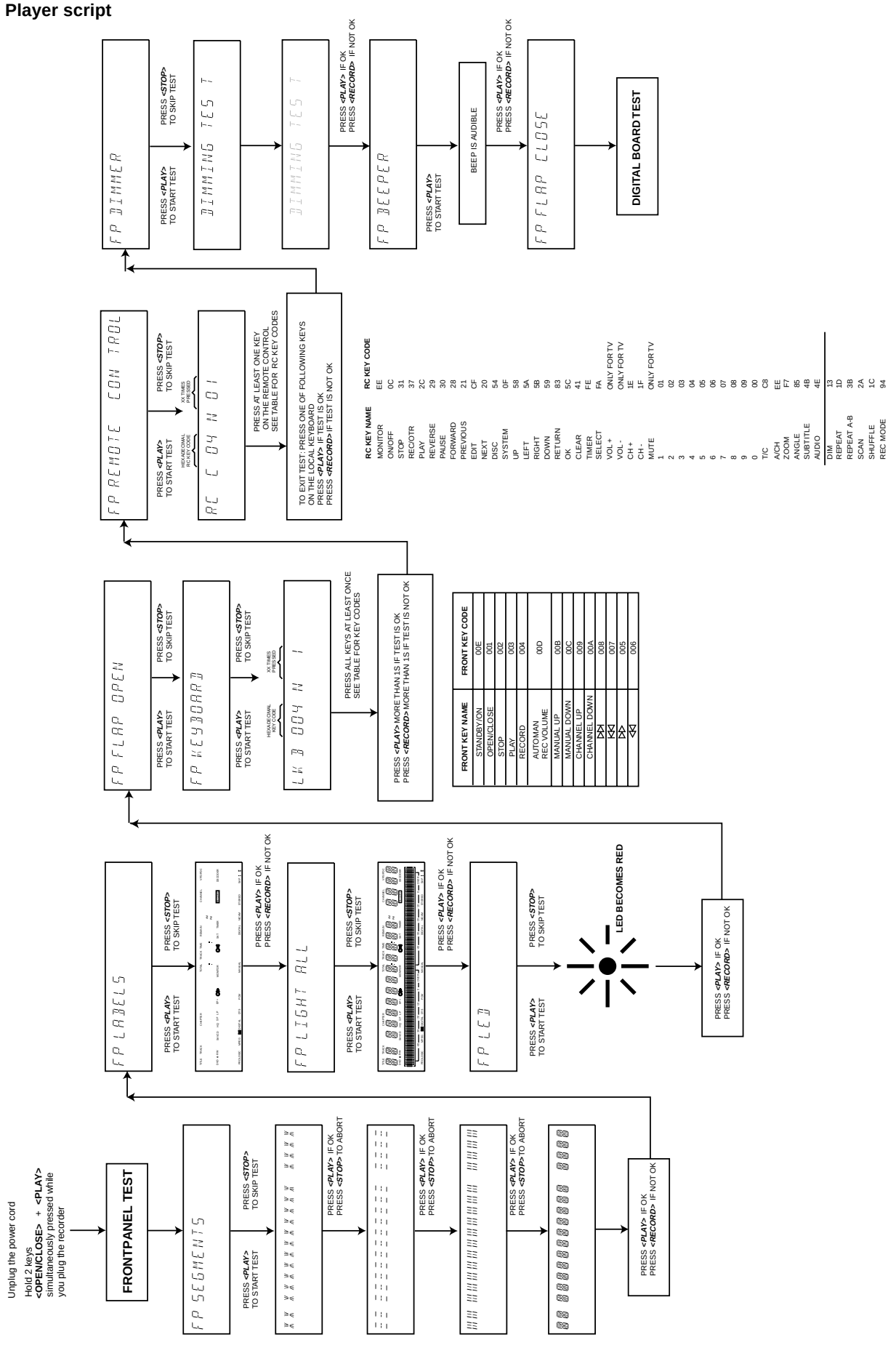


Fig. 2

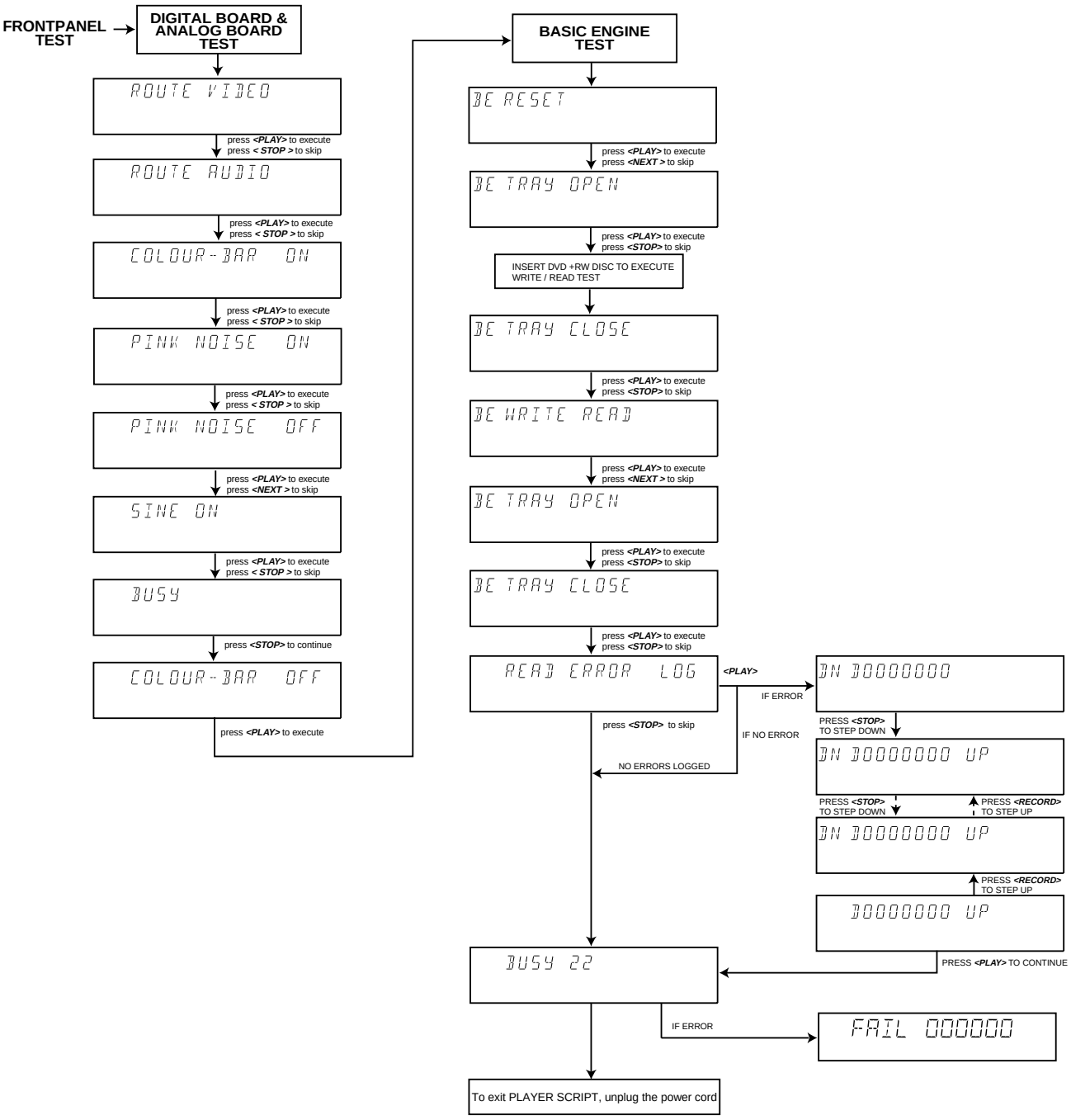


Fig. 3

2.3 Error Log

Explanation:

The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown

D error codes are identical to the Nuclei Error Codes (paragraph 4).

2.4 Trade Mode

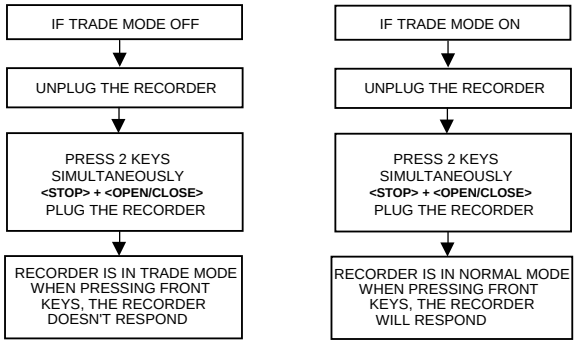

IF TRADE MODE OFF
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN TRADE MODE WHEN PRESSING FRONT KEYS, THE RECORDER DOESN'T RESPOND
IF TRADE MODE ON
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN NORMAL MODE WHEN PRESSING FRONT KEYS, THE RECORDER WILL RESPOND

Fig. 4

2.5 Virgin Mode

If you want that the recorder starts up in Virgin mode, follow this procedure:

- Unplug the recorder
- plug the recorder again while you keep the STAND BY/ ON key pressed
- the set starts up in Virgin mode.

3. Menu and Command Mode Interface

3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.

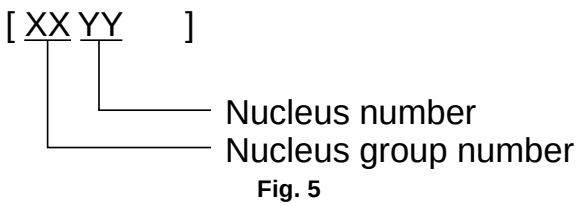


Fig. 5

The following groups are defined:

Group number	Group name
0	Basic / S cripts
1	Host decoder (Sti5508 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)
14	Miscellaneous

3.2 Error Handling

Each nucleus returns an error code. This code contains six numerals, which means:

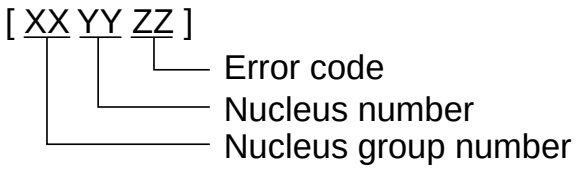


Fig. 6

The nucleus group numbers and nucleus numbers are the same as above.

3.3 Command Mode Interface

Set-Up Physical Interface Components

Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD recorder to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Code number of PC interface cable: 3122 785 90017

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```
DVD Video Recorder Diagnostic Software version 84
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu,  (C) ommand or (S) 2B-interface?   [M] : @ C ↵
DD:>
```

Fig. 7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Command Overview

We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xxyy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On
121	Colour-bar Off
122	NvramWrR
123	NvramI2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board
135	Video Test Signal On
136	Video Test Signal Off
137	Macrovision Off

Audio Video Decoder [02]

[xxyy] Number	Nuclei
200	Video Encoder I2C
202	SAA7118 I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts
207	Audio Encoder I2C
208	SAA7118 select input
209	Empress Version

VSM [03]

[xxyy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xxyy] Number	Nuclei
400	Reset
401	Read
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xxyy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Discbar
516	Discbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xxyy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information

Analog Board [07]

[xxyy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
720	Bargraph Level Adjustment
721	Clock correction
722	Clock reference
723	Re-virginise Recorder
724	Flash Checksum
725	Tuner frequency selection
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board
730	Store external presets
731	Get slash version
732	AFC Reference Voltage Tuner

DVIO [08]

[xxyy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids
805	Execute DVIO module SelfTest
806	Set DVIO led on.
807	Set DVIO led off.

Loop Nuclei [09]

[xxyy] Number	Nuclei
900	Digital Audio Loop
901	User / Dealer Audio Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop
906	User / Dealer Video Loop
907	User / Dealer Video VBI Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop
911	System Video Vip

Miscellanious [14]

[xxyy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off
1415	Progressive Scan Route Enable
1416	Progressive Scan Route Disable

Scripts [00]

[xxyy] Number	Nuclei
1 Us	erDealer Script
2 Pl	ayer Script

3.4 Menu Mode Interface

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```
DVD Video Recorder Diagnostic Software version 84
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu,  (C) ommand or (S) 2B-interface?   [M] : @ m  ↵

Main Menu

1.   Digital Board             ->
2.   Analog Board              ->
3.   Front Panel               ->
4.   Basic Engine              ->
5.   DVIO                      ->
6.   Progressive Scan Board    ->
7.   Loop tests                ->
8.   Log                       ->
9.   Scripts                   ->

Select>
```

Fig. 8

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

Menu Structure

The following menu structure is given after starting up the DVD recorder in menu mode. The symbol -> indicates that the current menu choice will invoke the display of a submenu.

Main Menu
1.Digital Board ->
2.Analogue Board ->
3.Front Panel ->
4.Basic Engine ->
5.DVIO ->
6.Progressive Scan Board ->
7.Loop Tests ->
8.Log ->
9.Scripts ->

Digital Board Menu
1.Host Decoder ->
2.VSM ->
3.AVENC ->
4.NVRAM ->

Host Decoder Menu
1.Flash Checksum
2.Flash1 Write Access
3.Flash2 Write Access
4.Flash Write/Read
5.Host SDRAM Write/Read
6.Host SDRAM Fast Write/Read
7.Host DRAM Write/Read
8.Host DRAM Fast Write/Read
9.I2C NVRAM
10.NVRAM Write/Read
11.Engine S2B Echo
12.Versions ->
13.Audio Mute ->
14.Colourbar ->
15.Pink Noise ->
16.Sine Generate ->

Digital Board Versions Menu
1.Hardware Version
2.Bootcode version
3.Applications Version
4.Diagnostics Version
5.Download Version

Audio Mute Menu
1.Audio Mute On
2.Audio Mute Off
Colourbar Menu
1.Colourbar On
2.Colourbar Off

Pink Noise Menu
1.Pink Noise On
2.Pink Noise Off

Sine Generate Menu
1.Sine On
2.Sine Burst 1kHz
3.Sine Burst 12kHz

VSM Menu
1.Register Access
2.SDRAM Access
3.VSM SDRAM Write/Read
4.Interrupt Lines
5.VSM Interconnection
6.UART

AVENC Menu
1.Empress ->
2.Video Input Processors ->

Empress Menu
1.Version number

Video Input Processors Menu
1.SAA7118 I2C Access

NVRAM Menu
1.Read Error Log
2.Reset Error Log
3.Read DVIO Unique ID

Analogue Board Menu
1.Echo
2.Obsolete
3.Route Video Input back to Digital board
4.Route Audio Input back to Digital board
5.Flash Checksum
6.Versions ->
7.Components ->
8.Re-virginize Recorder ->

Analogue Board Versions Menu
1.Hardware Version
2.Bootcode version
3.Application version
4.Diagnostics version
5.Download version

Analogue Components Menu
1.Tuner
2.Data Slicer
3.Sound Processor
4.AV Selector
5.NVRAM

Analogue Board Re-virginize Menu
1.Re-virginize Recorder
2.Set Virgin-bit
3.Clear Virgin-bit
4.Store external presets

Front Panel Menu
1.Echo
2.Version
3.Flap Control ->
4.Segment Test ->
5.Light Labels
6.Led test
7.Keyboard test
8.Remote Control
9.Beep
10.Disc Bar
11.Disc Bar Dots
12.Vu Grid
13.Dimmer
14.Blink
15.Light All Segments

Flap Control Menu
1.Open Flap
2.Close Flap

Segment Test Menu
1.Starburst
2.Light Horizontal Segments
3.Light Vertical Segments
4.Light All Segments

Basic Engine Menu
1.Reset
2.S2B Pass-through
3.S2B Echo
4.Focus On
5.Focus Off
6.Version
7.Self Test
8.Get Self Test Result
9.Basic Engine Test
10.Laser Test
11.Focus Test
12.Tilt Test
13.Optimise Jitter
14.Statistics Info
15.Log ->
16.Spindle Motor ->
17.Radial ->
18.Sledge ->
19.Tray ->

Basic Engine Error Log
1.Read Error Log
2.Reset Error Log

Basic Engine Spindle Motor Menu
1.Spindle Motor On
2.Spindle Motor Off
3.Spindle Motor Test

Basic Engine Radial Menu
1.Radial On
2.Radial Off
3.Radial Initialisation
4.Radial ATLS Calibration

Basic Engine Sledge Menu
1.Sledge test
2.Sledge test slow

Basic Engine Tray Menu
1.Tray In
2.Tray Out

DVIO Menu
1.Check Presence
2.Reset
3.Access
4.Error Codes
5.Module Identifiers
6.Led ->

DVIO Led Menu
1.Led On
2.Led Off

Progressive Scan Board Menu
1.I2C Access
2.Test Image On
3.Test Image Off

Loop Tests Menu
1.Digital Board Loops ->
2.User/Dealer Loops ->
3.System Loops ->
4.Basic Engine Loops ->

Digital Board Loops Menu
1.Obsolete
2.Digital Video Loop
3.Digital Video Loop VBI
User/Dealer Loops Menu
1.User/Dealer Audio Loop
2.User/Dealer Video Loop
3.User/Dealer Video Loop VBI

System Loops Menu
1.System Video Loop
2.System Video Loop VBI
3.System Audio Loop SCART(EURO)
4.System Audio Loop CINCH (NAFTA)

Basic Engine Loops Menu
1.Basic Engine write read
2.Basic Engine write read endless loop

Log Menu
1.Read Error Log
2.Reset Error Log

Script Menu
1.User/Dealer Script
2.Player Script

4. Nuclei Error Codes

In the following table the error codes will be described.

Error	Nr Error String
10000	“Checksum is OK”
10001	“segment name Checksum doesn’t match”” or “”seg-ment name segment not found”
10100	“”
10101	“FLASH 1 Write access test failed”
10200	“”
10201	“FLASH 2 Write access test failed”
10300	“”
10301	“FLASH write test failed”
10302	“FLASH write command failed”
10303	“FLASH write test done max. number of times”
10400	“”
10401	“HostDec SDRAM Memory data bus test goes wrong.”
10402	“ HostDec SDRAM Memory address bus test goes wrong.”
10403	“ HostDec SDRAM Physical memory device test goes wrong.”
10500	“”
10501	“ HostDec SDRAM Memory data bus test goes wrong.”
10502	“ HostDec SDRAM Memory address bus test goes wrong.”
10503	“ HostDec SDRAM Physical memory device test goes wrong.”
10600	“”
10601	“HostDec DRAM Memory data bus test goes wrong.”
10602	“HostDec DRAM Memory address bus test goes wrong.”
10603	“HostDec DRAM Physical memory device test goes wrong.”
10700	“”
10701	“HostDec DRAM Memory data bus test goes wrong.”
10702	“HostDec DRAM Memory address bus test goes wrong.”
10703	“HostDec DRAM Physical memory device test goes wrong.”
10800	“Host Decoder version(cut) number: version number””Digital hardware version”
10801	“Can not find version in FLASH.”
10900	“”
10901	“Error muting audio”
11000	“”
11001	“Error demuting audio”

Error	Nr Error String
11500	“”
11501	“Init of I2C failed”
11502	“The selection of the clock source failed”
11504	“The demute of the audio failed”
11600	“”
11601	“Init of I2C failed”
11602	“The mute of the audio failed”
11700	“”
11701	“Init of I2C failed”
11702	“The muting of the audio failed”
11703	“The demute of the audio failed”
11704	“The selection of the clock source failed”
11707	“Setup of Front panel failed”
11708	“Sine on Front panel keyboard failed”
11800	“”
11801	“Init of I2C failed”
11802	“The muting of the audio failed”
11803	“The demute of the audio failed”
11804	“The selection of the clock source failed”
11805	“Error cannot start VSM audio in port”
11900	“”
11901	“Init of I2C failed”
11902	“The muting of the audio failed”
11903	“The demute of the audio failed”
11904	“The selection of the clock source failed”
11905	“Error cannot start VSM audio in port”
12000	“”
12001	“Invalid input”
12100	“”
12200	“”
12201	“I2C bus busy before start”
12202	“NVRAM access time-out”
12203	“No NVRAM acknowledge”
12204	“NVRAM time-out”
12205	“NVRAM Write/Read back failed”
12300	“”
12301	“I2C bus busy before start”
12302	“NVRAM read access time-out”
12303	“No NVRAM read acknowledge”
12304	“NVRAM read failed”
13000	“Bootcode application version : bootversion”
13001	“Can not find version in FLASH.”
13100	“Recorder application version : recorderversion”
13101	“Can not find version in FLASH.”
13200	“Diagnostics application version : diagversion”
13201	“Can not find version in FLASH.”
13300	“Download application version : downloadversion”
13301	“Can not find version in FLASH.”

Error	Nr Error String
13700	“”
13701	“Turning off MacroVision failed”
20000	“”
20001	“I2C bus busy before start”
20002	“Video Encoder access time-out”
20003	“No acknowledge from Video Encoder”
20004	“No data send/received to or from Video Encoder”
20005	“SAA7118 VIP can not be initialised”
20200	“”
20201	“I2C bus busy before start”
20202	“SAA7118 VIP access time-out”
20203	“No acknowledge from SAA7118 VIP”
20204	“No data received from SAA7118 VIP”
20300	“”
20301	“Error audio encoder SRAM access cannot initial-ise I2C”
20302	“Error audio encoder SRAM access cannot reset DSP through I2C”
20303	“Error audio encoder SRAM access cannot down-load boot”
20304	“Error audio encoder cannot download test code”
20305	“Error audio encoder cannot obtain result of test”
20306	“Error audio encoder SRAM access stuck-at-zero data line “
20307	“Error audio encoder SRAM access stuck-at-one data line “
20308	“Error audio encoder SRAM access stuck-at-one address line “
20309	“Error audio encoder SRAM access address line address line x is connected to data line data line y”
20310	“Error audio encoder SRAM access address lines address line x and address line y are connected “
20311	“Error audio encoder SRAM access data lines data line x and data line y are connected “
20312	“Error audio encoder SRAM access illegal data re-ceived”
20400	“”
20401	“Error audio encoder access cannot initialise I2C”
20402	“Error audio encoder access cannot reset DSP through I2C”
20403	“Error audio encoder accessing ICR register”
20404	“Error audio encoder access stuck-at-zero of data line “
20405	“Error audio encoder access stuck-at-one of data line “
20406	“Audio encoder access data lines data line x and data line y are interconnected “

Error	Nr Error String
20500	“”
20501	“Error audio encoder SRAM WRR cannot initialise I2C”
20502	“Error audio encoder SRAM WRR cannot reset DSP through I2C”
20503	“Error audio encoder WRR cannot download boot”
20504	“Error audio encoder cannot download test code”
20505	“Error audio encoder SRAM WRR cannot obtain result of test”
20506	“Error audio encoder WRR SRAM stuck-at-zero data bit “
20507	“Error audio encoder WRR SRAM stuck-at-one data bit “
20508	“Error audio encoder WRR SRAM data lines data line x and data line y are connected”
20509	“Error audio encoder WRR SRAM illegal data re-ceived”
20600	“”
20601	“Error audio encoder interrupt cannot initialise I2C”
20602	“Error audio encoder interrupt cannot reset DSP through I2C”
20603	“Error audio encoder cannot download test code”
20604	“Error occurred accessing VSM”
20605	“Audio encoder interrupt not received”
20606	“Error occurred while activating the encoder”
20607	“Error audio encoder interrupt cannot initialise em-press”
20608	“Error occurred while getting interrupt reason”
20700	“”
20701	“Error audio encoder I2C cannot reset DSP through I2C”
20702	“Error audio encoder cannot download boot”
20703	“Error audio encoder cannot download TEST code”
20704	“Error audio encoder I2C bus busy”
20705	“Error audio encoder I2C cannot write slave ad-dress”
20706	“Error audio encoder I2C no acknowledge re-ceived”
20707	“Error audio encoder I2C cannot send/receive da-ta”
20708	“Error audio encoder received data through I2C was invalid”
20800	“”
20801	“I2C access failed.”
20802	“SAA7118 VIP can not be initialised.”
20803	“Invalid input”
20900	“B1.B2. B3.B4. B5.B6. B7.B8. B9.B10. B11.B12.”
20901	“Firmware download of EMPRESS failed”

Error	Nr Error String
20902	“I2C bus busy before start”
20903	“EMPRESS access time-out”
20904	“No acknowledge from the EMPRESS”
20905	“No data send to the EMPRESS”
20906	“No data received from the EMPRESS”
30000	“”
30001	“VSM SDRAM Bank1 Memory databus test goes wrong.”
30002	“VSM SDRAM Bank1 Memory addressbus test goes wrong.”
30003	“VSM SDRAM Bank1 Physical memory device test goes wrong.”
30004	“ VSM SDRAM Bank2 Memory databus test goes wrong.”
30005	“ VSM SDRAM Bank2 Memory addressbus test goes wrong.”
30006	“ VSM SDRAM Bank2 Physical memory device test goes wrong.”
30007	“VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:”
30008	“VSM SDRAM Bank2 VSM interrupt register A has a -stuck at- error for value:”
30100	“”
30101	“VSM SDRAM Bank1 Memory databus test goes wrong.”
30102	“VSM SDRAM Bank1 Memory addressbus test goes wrong.”
30103	“VSM SDRAM Bank1 Physical memory device test goes wrong.”
30104	“ VSM SDRAM Bank2 Memory databus test goes wrong.”
30105	“ VSM SDRAM Bank2 Memory addressbus test goes wrong.”
30106	“ VSM SDRAM Bank2 Physical memory device test goes wrong.”
30200	“”
30201	“VSM SDRAM Bank1 Memory databus test goes wrong.”
30202	“VSM SDRAM Bank1 Memory addressbus test goes wrong.”
30203	“VSM SDRAM Bank1 Physical memory device test goes wrong.”
30204	“ VSM SDRAM Bank2 Memory databus test goes wrong.”
30205	“ VSM SDRAM Bank2 Memory addressbus test goes wrong.”
30206	“ VSM SDRAM Bank2 Physical memory device test goes wrong.”
30300	“”
30301	“VSM interrupt register A has a -stuck at- error for value:”
30302	“VSM interrupt register B has a -stuck at- error for value:”
30303	“Interrupt A wasn’t raised.”

Error	Nr Error String
30304	“Interrupt B wasn’t raised.”
30305	“Interrupts A and B were raised.”
30400	“”
30401	“VSM SDRAM Bank1 Memory databus test goes wrong.”
30402	“VSM SDRAM Bank1 Memory addressbus test goes wrong.”
30403	“VSM SDRAM Bank1 Physical memory device test goes wrong.”
30404	“ VSM SDRAM Bank2 Memory databus test goes wrong.”
30405	“ VSM SDRAM Bank2 Memory addressbus test goes wrong.”
30406	“ VSM SDRAM Bank2 Physical memory device test goes wrong.”
30500	“”
30501	“Communication with the analogue board fails.”
30502	“Echo test to analogue board returned wrong string.”
40000	“”
40001	“NVRAM Reset; I2C failed”
40100	“NVRAM address = 0xaddress -> Byte value = 0xvalue”
40101	“NVRAM Read; I2C failed”
40102	“NVRAM Read; Invalid input”
40200	“”
40201	“NVRAM Modify; I2C failed”
40202	“NVRAM Modify; Invalid input”
40300	“DV Unique ID = id”
40301	“NVRAM Read DV Unique ID; I2C failed”
40400	“\r\n Error log:\r\n errorString \r\n “
40401	“NVRAM error log; I2C failed”
40402	“NVRAM error log is invalid”
40403	“Front panel failed”
40700	“”
40701	“NVRAM error log reset; I2C failed”
40900	“Region code Change counter is reset”
40901	“NVRAM region code reset; I2C failed”
41000	“”
41001	“NVRAM Store DV Unique ID; I2C failed”
41002	“NVRAM Store DV Unique ID; Invalid input”
50000	“”
50007	“Execution of the command on the analogue board failed.”
50008	“The frontpanel could not be accessed by the ana-logue board.”
50009	“The echo from the frontpanel processor was not correct.”
50100	“ Front panel version: FPversion “
50102	“Execution of the command on the analogue board failed.”

Error	Nr Error String
50103	“The frontpanel could not be accessed by the ana-logue board.”
50200	“”
50204	“Execution of the command on the analogue board failed.”
50205	“The frontpanel could not be accessed by the ana-logue board.”
50206	“The frontpanel did not show a starburst.”
50207	“The user skipped the FP-which pattern test.”
50208	“The user returned an unknown confirmation: con-firmation”
50209	“The frontpanel did not show horizontal segments.”
50210	“The frontpanel did not show vertical segments.”
50300	“”
50304	“Execution of the command on the analogue board failed.”
50305	“The frontpanel could not be accessed by the ana-logue board.”
50306	“The frontpanel did not light all labels.”
50307	“The user skipped the rest of the FP-label test.”
50308	“The user returned an unknown confirmation: con-firmation”
50400	“”
50404	“Execution of the command on the analogue board failed.”
50405	“The frontpanel could not be accessed by the ana-logue board.”
50406	“The LED’s could not be turned on.”
50407	“The user skipped the rest of the FP-LED test.”
50408	“The user returned an unknown confirmation: con-firmation”
50500	“”
50502	“Front panel Keyboard; test failed”
50503	“Front panel Keyboard; test aborted”
50504	“Front panel Keyboard; not all keys were pressed”
50505	“Front panel keyboard I2C connection failed”
50506	“Unable to get slashversion”
50600	“”
50602	“Front panel Remote control; test failed”
50603	“Front panel Remote control; test aborted”
50604	“Front panel remote control; can not access FP”
50605	“Front panel remote control; no user input received”
50700	“”
50701	“Execution of the command on the analogue board failed.”
50702	“The frontpanel could not be accessed by the ana-logue board.”

Error	Nr Error String
50703	“The frontpanel did not show a starburst.”
50704	“The user skipped the FP-starburst test.”
50705	“The user returned an unknown confirmation: con-firmation”
50800	“”
50801	“Execution of the command on the analogue board failed.”
50802	“The frontpanel could not be accessed by the ana-logue board.”
50803	“The frontpanel did not show vertical segments.”
50804	“The user skipped the FP-vertical segments test.”
50805	“The user returned an unknown confirmation: con-firmation”
50900	“”
50901	“Execution of the command on the analogue board failed.”
50902	“The frontpanel could not be accessed by the ana-logue board.”
50903	“The frontpanel did not show horizontal segments.”
50904	“The user skipped the FP-horizontal segments test.”
50905	“The user returned an unknown confirmation: con-firmation”
51400	“”
51401	“Execution of the command on the analogue board failed.”
51402	“The frontpanel could not be accessed by the ana-logue board.”
51403	“The beeper did not sound.”
51404	“The user skipped the FP-Beep test.”
51405	“The user returned an unknown confirmation: con-firmation”
51500	“”
51501	“Execution of the command on the analogue board failed.”
51502	“The frontpanel could not be accessed by the ana-logue board.”
51503	“The discbar did not display properly.”
51504	“The user skipped the discbar test.”
51505	“The user returned an unknown confirmation: con-firmation”
51600	“”
51601	“Execution of the command on the analogue board failed.”
51602	“The frontpanel could not be accessed by the ana-logue board.”
51603	“The discbar dots did not display properly.”
51604	“The user skipped the discbar dots test.”
51605	“The user returned an unknown confirmation: con-firmation”
51700	“”

Error	Nr Error String
51701	“Execution of the command on the analogue board failed.”
51702	“The frontpanel could not be accessed by the ana-logue board.”
51703	“The VU grid did not display properly.”
51704	“The user skipped the VU gridtest.”
51705	“The user returned an unknown confirmation: con-firmation”
51800	“”
51801	“Execution of the command on the analogue board failed.”
51802	“The frontpanel could not be accessed by the ana-logue board.”
51803	“The frontpanel could not be dimmed.”
51804	“The user skipped the FP-Dim test.”
51805	“The user returned an unknown confirmation: con-firmation”
51900	“”
51901	“Execution of the command on the analogue board failed.”
51902	“The frontpanel could not be accessed by the ana-logue board.”
51903	“The frontpanel did not show segments blinking.”
51904	“The user skipped the FP-blinking test.”
51905	“The user returned an unknown confirmation: con-firmation”
52000	“”
52001	“Execution of the command on the analogue board failed.”
52002	“The frontpanel could not be accessed by the ana-logue board.”
52003	“The frontpanel did not show all segments lit.”
52004	“The user skipped the FP-light all segments test.”
52005	“The user returned an unknown confirmation: con-firmation”
52200	“”
52201	“Communication with Analogue Board fails.”
52202	“Frontpanel can not be accessed by the Analogue Board.”
52300	“”
52301	“Communication with Analogue Board fails.”
52302	“Frontpanel can not be accessed by the Analogue Board.”
60000	“”
60100	“”
60101	“Basic Engine returned error number 0xerrornumber”
60102	“Parity error from Basic Engine to Serial”
60103	“Communication time-out error”
60104	“Unexpected response from Basic Engine”
60105	“Echo loop could not be closed”

Error	Nr Error String
60106	“Wrong echo pattern received”
60200	“Version: nr1.nr2.nr3”
60201	“Basic Engine returned error number 0xerrornumber”
60202	“Parity error from Basic Engine to Serial”
60203	“Communication time-out error”
60204	“Unexpected response from Basic Engine”
60205	“Front Panel failed.”
60300	“”
60301	“Basic-Engine time-out error”
60400	“”
60401	“Basic Engine returned error number 0xerrornumber”
60402	“Parity error from Basic Engine to Serial”
60403	“Communication time-out error”
60404	“Unexpected response from Basic Engine”
60405	“Focus loop could not be closed”
60500	“”
60501	“Basic Engine returned error number 0xerrornumber”
60502	“Parity error from Basic Engine to Serial”
60503	“Communication time-out error”
60504	“Unexpected response from Basic Engine”
60600	“”
60601	“Basic Engine returned error number 0xerrornumber”
60602	“Parity error from Basic Engine to Serial”
60603	“Communication time-out error”
60604	“Unexpected response from Basic Engine”
60700	“”
60701	“Basic Engine returned error number 0xerrornumber”
60702	“Parity error from Basic Engine to Serial”
60703	“Communication time-out error”
60704	“Unexpected response from Basic Engine”
60800	“”
60801	“Basic Engine returned error number 0xerrornumber”
60802	“Parity error from Basic Engine to Serial”
60803	“Communication time-out error”
60804	“Unexpected response from Basic Engine”
60805	“Radial loop could not be closed”
60900	“”
60901	“Basic Engine returned error number 0xerrornumber”
60902	“Parity error from Basic Engine to Serial”
60903	“Communication time-out error”
60904	“Unexpected response from Basic Engine”
61500	“”
61501	“Basic Engine returned error number 0xerrornumber”

Error	Nr Error String
61502	“Parity error from Basic Engine to Serial”
61503	“Communication time-out error”
61504	“Unexpected response from Basic Engine”
61600	“”
61601	“Basic Engine returned error number 0xerrornumber”
61602	“Parity error from Basic Engine to Serial”
61603	“Communication time-out error”
61604	“Unexpected response from Basic Engine”
61700	“”
61701	“BE tray-in command failed”
61702	“BE read-TOC command failed”
61703	“BE VSM interrupt initialisation failed”
61704	“BE set irq command failed”
61705	“BE no disc or wrong disc inserted”
61706	“BE rec-pause command failed”
61707	“BE VSM BE out DMA initialisation failed”
61708	“BE VSM BE out initialisation failed”
61709	“BE VSM BE out DMA start failed”
61710	“BE VSM BE out start failed”
61711	“BE rec command failed”
61712	“BE VSM out underrun error occurred”
61713	“BE record complete interrupt not raised”
61714	“BE get irq command failed”
61715	“BE no interrupt was raised by BE”
61716	“BE VSM DMA out not finished”
61717	“BE stop command after writing failed”
61718	“BE VSM Sector processor initialisation failed”
61719	“BE VSM sector processor DMA initialisation failed”
61720	“BE VSM sector processor DMA start failed”
61721	“BE VSM sector processor start failed”
61722	“BE seek command failed”
61723	“BE VSM sector processor error occurred”
61724	“BE read timeout occurred”
61725	“BE stop command after reading failed”
61726	“BE difference found in data at disc sector 0xdiscsector”
61727	“This nucleus cannot be executed because the Self-Test failed”
61800	“”
61801	“BE i2c initialisation failed”
61802	“This nucleus cannot be executed because the Self-Test failed”
61900	“”
61901	“The SelfTest failed with result: 0xnr1 0xnr2 0xnr3”
61902	“Basic Engine returned error number 0xerrornumber”
61903	“Parity error from Basic Engine to Serial”
61904	“Communication time-out error”

Error	Nr Error String
61905	“Unexpected response from Basic Engine”
62000	“”
62001	“Self-Test : errorstring1 Laser-Test : errorstring2 SpindleM-Test: errorstring3 Sledg-eM-Test : errorstring4 Focus-Test : errorstring5”
62100	“The forward sense level is 0xlevel”
62101	“Basic Engine returned error number 0xerrornumber”
62102	“Parity error from Basic Engine to Serial”
62103	“Communication time-out error”
62104	“Unexpected response from Basic Engine”
62200	“”
62201	“The BE-self-diagnostic-spindle-motor-test failed”
62202	“Basic Engine returned error number 0xerrornumber”
62203	“Parity error from Basic Engine to Serial”
62204	“Communication time-out error”
62205	“Unexpected response from Basic Engine”
62300	“”
62301	“The BE-focus-test failed”
62302	“Basic Engine returned error number 0xerrornumber”
62303	“Parity error from Basic Engine to Serial”
62304	“Communication time-out error”
62305	“Unexpected response from Basic Engine”
62400	“”
62401	“The BE-self-diagnostic-sledge-motor-test failed”
62402	“Basic Engine returned error number 0xerrornumber”
62403	“Parity error from Basic Engine to Serial”
62404	“Communication time-out error”
62405	“Unexpected response from Basic Engine”
62500	“”
62600	“”
62700	“BE EEPROM address = address -> Byte value = 0xvalue”
62701	“Basic Engine returned error number 0xerrornumber”
62702	“Parity error from Basic Engine to Serial”
62703	“Communication time-out error”
62704	“Unexpected response from Basic Engine”
62705	“BE read EEPROM; invalid input”
62800	“”
62801	“Basic Engine returned error number 0xerrornumber”
62802	“Parity error from Basic Engine to Serial”
62803	“Communication time-out error”
62804	“Unexpected response from Basic Engine”
62805	“BE write EEPROM; invalid input”

Error	Nr Error String
62900	“”
62901	“Basic Engine returned error number 0xerrornumber”
62902	“Parity error from Basic Engine to Serial”
62903	“Communication time-out error”
62904	“Unexpected response from Basic Engine”
62905	“Radial loop could not be closed”
63000	“”
63001	“Basic Engine returned error number 0xerrornumber”
63002	“Parity error from Basic Engine to Serial”
63003	“Communication time-out error”
63004	“Unexpected response from Basic Engine”
63100	“ Number of times Tray went Open/Closed : nr1”” Total hours the CD laser was on : nr2”” Total hours the DVD laser was on : nr3”” Total hours the write laser was on : nr4"
63101	“Basic Engine returned error number 0xerrornumber”
63102	“Parity error from Basic Engine to Serial”
63103	“Communication time-out error”
63104	“Unexpected response from Basic Engine”
63200	“”
63201	“Basic Engine returned error number 0xerrornumber”
63202	“Parity error from Basic Engine to Serial”
63203	“Communication time-out error”
63204	“Unexpected response from Basic Engine”
63300	Momentary errors (Byte 1 - Byte 7) : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Cumulative errors (Byte 1 - Byte 7): : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest) : : 0xb1 0xb2 0xb3 0xb4 0xb5
63301	“Basic Engine returned error number 0xerrornumber”
63302	“Parity error from Basic Engine to Serial”
63303	“Communication time-out error”
63304	“Unexpected response from Basic Engine”
63400	“”
63401	“Basic Engine returned error number 0xerrornumber”
63402	“Parity error from Basic Engine to Serial”
63403	“Communication time-out error”
63404	“Unexpected response from Basic Engine”
63500	“”
63501	“Basic Engine returned error number 0xerrornumber”
63502	“Parity error from Basic Engine to Serial”
63503	“Communication time-out error”
63504	“Unexpected response from Basic Engine”
63505	“errorstring _the basic engine will reject all player commands”
63900	“”

Error	Nr Error String
63901	“Basic Engine returned error number 0xerrornumber”
63902	“Parity error from Basic Engine to Serial”
63903	“Communication time-out error”
63904	“Unexpected response from Basic Engine”
64000	“BE OPU number = opunumber”
64001	“Basic Engine returned error number 0xerrornumber”
64002	“Parity error from Basic Engine to Serial”
64003	“Communication time-out error”
64004	“Unexpected response from Basic Engine”
64100	“The data was successfully written on and read from a DVD disc”
64101	“The tray-in command failed”
64102	“The read-TOC command failed”
64103	“The VSM interrupt initialisation failed”
64104	“The set irq command failed”
64105	“No disc or wrong disc inserted”
64106	“The rec-pause command failed”
64107	“The VSM BE out DMA initialisation failed”
64108	“The VSM BE out initialisation failed”
64109	“The VSM BE out DMA start failed”
64110	“The VSM BE out start failed”
64111	“The rec command failed”
64112	“The VSM out underrun error occurred”
64113	“The record complete interrupt was not raised”
64114	“The get irq command failed”
64115	“There was no interrupt raised by BE”
64116	“The VSM DMA did not finished”
64117	“The stop command after writing failed”
64118	“The VSM Sector processor initialisation failed”
64119	“The VSM sector processor DMA initialisation failed”
64120	“The VSM sector processor DMA start failed”
64121	“The VSM sector processor start failed”
64122	“The seek command failed”
64123	“The VSM sector processor error occurred”
64124	“The read timeout occurred”
64125	“The stop command after reading failed”
64126	“There was a difference found in data at a specific disc sector”
64127	“The result of the self test contains errors”
64128	“An error interrupt was raised by BE”
64129	“The calibrate-record command failed”
64130	“To many retries”
64131	“BE update RAI command after writing failed”
64132	“BE find first recordable address command failed”
64133	“DVD+R disc is full”
64200	“”

Error	Nr Error String
64201	“BE i2c initialisation failed”
64202	“This nucleus cannot be executed because the Self-Test failed”
70000	“Echo test OK”
70001	“Echo test returned wrong string.”
70002	“Communication with Analogue Board fails”
70300	“SoftwareVersion”
70301	“Can not find segment in FLASH ROM on the Ana-logue Board”
70302	“Communication with Analogue Board fails”
70400	“HardwareVersion”
70401	“Can not find segment in FLASH ROM on the Ana-logue Board”
70402	“Communication with Analogue Board fails”
70500	“Clock adjusted OK”
70501	“Can not adjust the clock on the Analogue Board.”
70502	“Wrong date/time text size.”
70503	“Communication with Analogue Board fails”
70600	“Tuner accessibility test OK”
70601	“Can not access tuner on the Analogue Board.”
70602	“Communication with Analogue Board fails”
70700	“Frequency download OK”
70701	“Wrong frequency table size.”
70702	“Can not download the frequency table into the an-alogue NVRAM.”
70703	“Can not download the frequency table into the an-alogue NVRAM.”
70704	“Communication with Analogue Board fails”
70800	“Data slicer test OK”
70801	“Test of the Data slicer on the Analogue Board fails.”
70802	“Communication with Analogue Board fails”
70900	“Sound Processor test OK”
70901	“Test of the Sound Processor on the Analogue Board fails.”
70902	“Communication with Analogue Board fails”
71000	“AV Selector test OK”
71001	“Test of the AV Selector on the Analogue Board fails.”
71002	“Communication with Analogue Board fails”
71100	“NVRAM test OK”
71101	“Test of the NVRAM on the Analogue Board fails.”
71102	“Communication with Analogue Board fails”
71200	“Video routing on the Analogue Board OK”
71201	“Routing the video on the Analogue Board fails.”
71202	“Invalid input.”
71203	“Communication with Analogue Board fails”
71300	“Audio routing on the Analogue Board OK”

Error	Nr Error String
71301	“Routing the audio on the Analogue Board fails.”
71302	“Invalid input.”
71303	“Communication with Analogue Board fails”
71500	“”
71501	“Invalid slash version, default slash version is set.”
71502	“Setting the slash version on the Analogue Board fails.”
71503	“Communication with Analogue Board fails”
71600	“ApplicationVersion”
71601	“Can not find segment in FLASH ROM on the Ana-logue Board”
71602	“Communication with Analogue Board fails”
71700	“DiagnosticsVersion”
71701	“Can not find segment in FLASH ROM on the Ana-logue Board”
71702	“Communication with Analogue Board fails”
71800	“DownloadVersion”
71801	“Can not find segment in FLASH ROM on the Ana-logue Board”
71802	“Communication with Analogue Board fails”
72300	“”
72000	“”
72001	“Adjusting BarGraphLevel failed”
72002	“Communication with Analogue Board fails”
72100	“”
72101	“Storing clock correction failed”
72102	“Value out of range : default value stored “
72103	“Invalid input.”
72104	“Communication with Analogue Board fails”
72200	“”
72201	“Initialising the 1Hz signal on the Clock IC failed”
72202	“Communication with Analogue Board fails”
72301	“Clearing the NVRAM on the Analogue Board fails”
72302	“Communication with Analogue Board fails”
72400	“segment checksum is : checksum which is cor-rect”” for every segment”
72401	“segment could not be found”” or “”segment check-sum is : checksumC ,however it should be : check-sumE”” for every segment”
72402	“Communication with Analogue Board fails”
72900	“Date received”
72901	“Data returned”
72902	“Communication on I2C-bus failed on the Ana-logue Board fails.”
72903	“Communication with Analogue Board fails”
73000	“”
73001	“Storing the external presets on the Analogue Board fails”

Error	Nr Error String
73002	“Communication with Analogue Board fails”
73100	“0xslashversion”” where slashversion is the slash version read from the analogue board”
73101	“Error while reading out slash version.”
73102	“I2C Write error.”
73103	“I2C Read error.”
73104	“Communication with Analogue Board fails”
73200	“”
73201	“Storing the Reference Voltage for the Tuner failed”
73202	“Invalid input.”
73203	“Communication with Analogue Board fails”
80000	“The DVIO module is present in the system.”
80001	“The DVIO module is not present in the system.”
80100	“The DVIO module has been reset OK.”
80101	“The DVIO module is not present in the system.”
80102	“The DVIO module could not be reset.”
80103	“Could not initialise I2C before Reset.”
80200	“The accessibility of the DVIO module is OK.”
80201	“The DVIO board is not present in this DVDR.”
80202	“Could not initialise I2C.”
80203	“Unable to reset the DVIO module.”
80204	“Unable to receive the reset indication from the DVIO module.”
80205	“Unable to send the configuration to the DVIO module.”
80206	“Unable to download the chip ID to the DVIO mod-ule.”
80207	“Unable to set the mode of the DVIO module to IDLE.”
80208	“Software Error in function HandleStateAwaitin-gReply!!”
80209	“Maximal number of retries reached by HandleS-tateSending!!”
80210	“Maximal number of retries (NACKs) reached (HandleStateSending)”
80211	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!”
80212	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!”
80213	“We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!”
80214	“VSM UART error timeout transmitting command”
80215	“VSM UART error timeout receiving reply”
80216	“VSM UART frame error occurred receiving from DVIO board”
80217	“VSM UART parity error occurred receiving from DVIO board”
80218	“The confirmation/indication from the DVIO module is invalid.”

Error	Nr Error String
80300	“The accessibility of the DVIO module is OK.”
80301	“The DVIO board is not present in this DVDR.”
80302	“Could not initialise I2C.”
80303	“Unable to reset the DVIO module.”
80304	“Unable to receive the reset indication from the DVIO module.”
80305	“Unable to send the configuration to the DVIO module.”
80306	“Unable to download the chip ID to the DVIO mod-ule.”
80307	“Unable to set the mode of the DVIO module to IDLE.”
80308	“Software Error in function HandleStateAwaitin-gReply!!”
80309	“Maximal number of retries reached by HandleS-tateSending!!”
80310	“Maximal number of retries (NACKs) reached (HandleStateSending)”
80311	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!”
80312	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!”
80313	“We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!”
80314	“VSM UART error timeout transmitting command”
80315	“VSM UART error timeout receiving reply”
80316	“VSM UART frame error occurred receiving from DVIO board”
80317	“VSM UART parity error occurred receiving from DVIO board”
80318	“The confirmation/indication from the DVIO module is invalid.”
80400	“The accessibility of the DVIO module is OK.”
80401	“The DVIO board is not present in this DVDR.”
80402	“Could not initialise I2C.”
80403	“Unable to reset the DVIO module.”
80404	“Unable to receive the reset indication from the DVIO module.”
80405	“Unable to send the configuration to the DVIO module.”
80406	“Unable to download the chip ID to the DVIO mod-ule.”
80407	“Unable to set the mode of the DVIO module to IDLE.”
80408	“Software Error in function HandleStateAwaitin-gReply!!”
80409	“Maximal number of retries reached by HandleS-tateSending!!”
80410	“Maximal number of retries (NACKs) reached (HandleStateSending)”
80411	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!”

Error	Nr Error String
80412	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!”
80413	“We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!”
80414	“VSM UART error timeout transmitting command”
80415	“VSM UART error timeout receiving reply”
80416	“VSM UART frame error occurred receiving from DVIO board”
80417	“VSM UART parity error occurred receiving from DVIO board”
80418	“The confirmation/indication from the DVIO module is invalid.”
80500	“”
80501	“The DVIO board is not present in this DVDR.”
80502	“The I2C could not be initialised.”
80503	“The DVIO module could not be reset.”
80504	“Unable to receive the reset indication from the DVIO module.”
80505	“Unable to send the configuration to the DVIO module.”
80506	“Unable to download the chip ID to the DVIO mod-ule.”
80507	“Unable to set the mode of the DVIO module to IDLE.”
80508	“Software Error in HandleStateAwaitingReply func-tion!”
80509	“Maximal number of retries reached by HandleS-tateSending!”
80510	“Maximal number of retries (NACK’s) reached “”(HandleStateSending)”
80511	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!”
80512	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!”
80513	“We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!”
80514	“VSM UART error timeout transmitting command”
80515	“VSM UART error timeout receiving reply”
80516	“VSM UART frame error occurred receiving from DVIO board”
80517	“VSM UART parity error occurred receiving from DVIO board”
80518	“The confirmation/indication from the DVIO module is invalid.”
80519	“Setting the DVIO module in/out diagnostics mode failed”
80520	“Invalid input”
80521	“Getting the errors of the self-test failed”
80522	“Self-test failed”
80600	“”
80601	“The DVIO board is not present in this DVDR.”
80602	“The I2C could not be initialised.”

Error	Nr Error String
80603	“The DVIO module could not be reset.”
80604	“Unable to receive the reset indication from the DVIO module.”
80605	“Unable to send the configuration to the DVIO module.”
80606	“Unable to download the chip ID to the DVIO mod-ule.”
80607	“Unable to set the mode of the DVIO module to IDLE.”
80608	“Software Error in HandleStateAwaitingReply func-tion!”
80609	“Maximal number of retries reached by HandleS-tateSending!”
80610	“Maximal number of retries (NACK’s) reached “”(HandleStateSending)”
80611	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!”
80612	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!”
80613	“We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!”
80614	“VSM UART error timeout transmitting command”
80615	“VSM UART error timeout receiving reply”
80616	“VSM UART frame error occurred receiving from DVIO board”
80617	“VSM UART parity error occurred receiving from DVIO board”
80618	“The confirmation/indication from the DVIO module is invalid.”
80619	“Setting the DVIO module in/out diagnostics mode failed”
80700	“”
80701	“The DVIO board is not present in this DVDR.”
80702	“The I2C could not be initialised.”
80703	“The DVIO module could not be reset.”
80704	“Unable to receive the reset indication from the DVIO module.”
80705	“Unable to send the configuration to the DVIO module.”
80706	“Unable to download the chip ID to the DVIO mod-ule.”
80707	“Unable to set the mode of the DVIO module to IDLE.”
80708	“Software Error in HandleStateAwaitingReply func-tion!”
80709	“Maximal number of retries reached by HandleS-tateSending!”
80710	“Maximal number of retries (NACK’s) reached “”(HandleStateSending)”
80711	“We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!”
80712	“We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!”

Error	Nr Error String
80713	“We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!”
80714	“VSM UART error timeout transmitting command”
80715	“VSM UART error timeout receiving reply”
80716	“VSM UART frame error occurred receiving from DVIO board”
80717	“VSM UART parity error occurred receiving from DVIO board”
80718	“The confirmation/indication from the DVIO module is invalid.”
80719	“Setting the DVIO module in/out diagnostics mode failed”
90121	“Error: audio data in host memory contains wrong frequency: frequency Hz”
90122	“Error: audio data in host memory contains si-lence!”
90123	“There is no correct audio frame in the buffer”
90124	“The audio frame has an illegal version bit”
90125	“The audio frame has an illegal bitrate-index”
90126	“The audio frame has an illegal sampling rate”
90127	“The CRC of the audio frame is wrong”
90128	“The audio frame is not MPEG-I layer II !”
90129	“Error cannot de-mute DAC on analogue board”
90200	“”
90201	“Initialisation of I2C failed”
90202	“Initialisation of VIP and EMPIRE failed”
90203	“Initialisation of PLL / Link failed.”
90204	“Next descriptor address set wrong.”
90205	“Turning on the colourbar failed”
90206	“No I2C communication possible to start video en-coder.”
90207	“Starting the video encoder failed.”
90208	“Transfer of data from video encoder to VSM failed.”
90209	“Stopping the encoder failed.”
90210	“Turning off the colourbar failed.”
90211	“Cannot intialize hostdecoder parallel input”
90212	“Cannot initialise VSM AV-out DMA port”
90213	“Cannot initialise VSM AV-out port”
90214	“Cannot start VSM AV-out DMA port”
90215	“Cannot start VSM AV-out port”
90216	“Transfer of data from VSM to host decoder failed.”
90217	“VSM and Hostdec memory do not match (com-pared after transfer)”
90218	“Decoding of the video data in the hostdecoder memory failed”
90219	“The data in the hostdecoder is not equal to a col-ourbar”
90220	“The video encoder did not return the Group Of Picture count.”

Error	Nr Error String
90221	“The video encoder did not receive data from the VIP.”
90223	“Initialisation of VIP and EMPRESS failed”
90224	“The video encoder did not return the current sta-tus.”
90225	“The video encoder timed out in BUSY mode. (no VIP input)”
90226	“The video encoder did not return the current bi-trate.”
90227	“The video encoder did not switch to ENCODING mode.”
90228	“The video encoder could not start from STOP/ IDLE mode.”
90229	“The video encoder did not switch from IDLE to STOP mode.”
90300	“”
90301	“Initialisation of I2C failed”
90302	“I2C communication to VIP failed”
90303	“Initialisation of VIP failed”
90304	“Generation of Close Caption data failed”
90305	“VIP not locked to video signal”
90306	“Initialisation of VBI Extractor failed”
90307	“No CC data received”
90308	“Closed Caption data overrun”
90309	“Closed Caption data does not match”
90310	“Switch off ColourBar failed”
90400	“”
90401	“Initialisation of I2C failed”
90402	“Initialisation of VIP and EMPIRE failed”
90403	“Initialisation of PLL / Link failed.”
90404	“Next descriptor address set wrong.”
90405	“Turning on the colourbar failed”
90406	“No I2C communication possible to start video en-coder.”
90407	“Starting the video encoder failed.”
90408	“Transfer of data from video encoder to VSM failed.”
90409	“Stopping the encoder failed.”
90410	“Turning off the colourbar failed.”
90411	“Cannot intialize hostdecoder parallel input”
90412	“Cannot initialise VSM AV-out DMA port”
90413	“Cannot initialise VSM AV-out port”
90414	“Cannot start VSM AV-out DMA port”
90415	“Cannot start VSM AV-out port”
90416	“Transfer of data from VSM to host decoder failed.”
90417	“VSM and Hostdec memory do not match (com-pared after transfer)”
90418	“Decoding of the video data in the hostdecoder memory failed”
90419	“The data in the hostdecoder is not equal to a col-ourbar”

Error	Nr Error String
90420	“The video encoder did not return the Group Of Picture count.”
90421	“The video encoder did not receive data from the VIP.”
90422	“Execution of the command on the analogue board failed.”
90423	“Initialisation of VIP and EMPRESS failed”
90424	“The video encoder did not return the current sta-tus.”
90425	“The video encoder timed out in BUSY mode. (no VIP input)”
90426	“The video encoder did not return the current bi-trate.”
90427	“The video encoder did not switch to ENCODING mode.”
90428	“The video encoder could not start from STOP/IDLE mode.”
90429	“The video encoder did not switch from IDLE to STOP mode.”
90500	“”
90501	“Initialisation of I2C failed”
90502	“I2C communication to VIP failed”
90503	“Initialisation of VIP failed”
90504	“Generation of Close Caption data failed”
90505	“VIP not locked to video signal”
90506	“Initialisation of VBI Extractor failed”
90507	“No CC data received”
90508	“Closed Caption data overrun”
90509	“Closed Caption data does not match”
90510	“Switch off ColourBar failed”
90511	“Execution of the command on the analogue board failed.”
90600	“”
90601	“Initialisation of I2C failed”
90602	“Initialisation of VIP and EMPIRE failed”
90603	“Initialisation of PLL / Link failed.”
90604	“Next descriptor address set wrong.”
90605	“Turning on the colourbar failed”
90606	“No I2C communication possible to start video en-coder.”
90607	“Starting the video encoder failed.”
90608	“Transfer of data from video encoder to VSM failed.”
90609	“Stopping the encoder failed.”
90610	“Turning off the colourbar failed.”
90611	“Cannot intialize hostdecoder parallel input”
90612	“Cannot initialise VSM AV-out DMA port”
90613	“Cannot initialise VSM AV-out port”
90614	“Cannot start VSM AV-out DMA port”
90615	“Cannot start VSM AV-out port”
90616	“Transfer of data from VSM to host decoder failed.”

Error	Nr Error String
90617	“VSM and Hostdec memory do not match (com-pared after transfer)”
90618	“Decoding of the video data in the hostdecoder memory failed”
90619	“The data in the hostdecoder is not equal to a col-ourbar”
90620	“The video encoder did not return the Group Of Picture count.”
90621	“The video encoder did not receive data from the VIP.”
90622	“Execution of the command on the analogue board failed.”
90623	“Initialisation of VIP and EMPRESS failed”
90624	“The video encoder did not return the current sta-tus.”
90625	“The video encoder timed out in BUSY mode. (no VIP input)”
90626	“The video encoder did not return the current bi-trate.”
90627	“The video encoder did not switch to ENCODING mode.”
90628	“The video encoder could not start from STOP/IDLE mode.”
90629	“The video encoder did not switch from IDLE to STOP mode.”
90700	“”
90701	“Initialisation of I2C failed”
90702	“I2C communication to VIP failed”
90703	“Initialisation of VIP failed”
90704	“Generation of Close Caption data failed”
90705	“VIP not locked to video signal”
90706	“Initialisation of VBI Extractor failed”
90707	“No CC data received”
90708	“Closed Caption data overrun”
90709	“Closed Caption data does not match”
90710	“Switch off ColourBar failed”
90711	“Execution of the command on the analogue board failed.”
90800	“”
90801	“Error routing the audio back to the digital board.”
90802	“Error cannot initialise I2C”
90803	“Error cannot initialise VIP”
90804	“Error cannot set ADC enable pin”
90805	“Error cannot set VSM audio clock”
90806	“Error preparing the 12kHz audio-sine”
90807	“Error cannot initialise audio encoder”
90808	“Error cannot initialise VSM audio in port”
90809	“Error cannot initialise VSM audio in DMA port”
90810	“Error cannot initialise VSM audio out DMA port”
90811	“Error cannot initialise audio VSM out port”

Error	Nr Error String
90812	“Error cannot initialise host decoder audio in”
90813	“Error loop audio user/dealer cannot start audio en-coder”
90814	“Error cannot start VSM audio in DMA port”
90815	“Error starting the 12kHz audio-sine”
90816	“Error transfer data from audio encoder to VSM”
90817	“Error cannot start VSM AV out DMA port”
90818	“Error cannot start VSM AV out port”
90819	“Error transfer data from VSM to host decoder”
90820	“Error: audio data in host memory and VSM mem-ory differ”
90821	“Error: audio data in host memory contains wrong frequency: frequency Hz”
90822	“Error: audio data in host memory contains si-lence!”
90823	“There is no correct audio frame in the buffer”
90824	“The audio frame has an illegal version bit”
90825	“The audio frame has an illegal bitrate-index”
90826	“The audio frame has an illegal sampling rate”
90827	“The CRC of the audio frame is wrong”
90828	“The audio frame is not MPEG-I layer II !”
90829	“Error cannot de-mute DAC on analogue board”
90900	“”
90901	“Error routing the audio back to the digital board.”
90902	“Error cannot initialise I2C”
90903	“Error cannot initialise VIP”
90904	“Error cannot set ADC enable pin”
90905	“Error cannot set VSM audio clock”
90906	“Error preparing the 12kHz audio-sine”
90907	“Error cannot initialise audio encoder”
90908	“Error cannot initialise VSM audio in port”
90909	“Error cannot initialise VSM audio in DMA port”
90910	“Error cannot initialise VSM audio out DMA port”
90911	“Error cannot initialise audio VSM out port”
90912	“Error cannot initialise host decoder audio in”
90913	“Error loop audio user/dealer cannot start audio en-coder”
90914	“Error cannot start VSM audio in DMA port”
90915	“Error starting the 12kHz audio-sine”
90916	“Error transfer data from audio encoder to VSM”
90917	“Error cannot start VSM AV out DMA port”
90918	“Error cannot start VSM AV out port”
90919	“Error transfer data from VSM to host decoder”

Error	Nr Error String
90920	“Error: audio data in host memory and VSM mem-ory differ”
90921	“Error: audio data in host memory contains wrong frequency: frequency Hz”
90922	“Error: audio data in host memory contains si-lence!”
90923	“There is no correct audio frame in the buffer”
90924	“The audio frame has an illegal version bit”
90925	“The audio frame has an illegal bitrate-index”
90926	“The audio frame has an illegal sampling rate”
90927	“The CRC of the audio frame is wrong”
90928	“The audio frame is not MPEG-I layer II !”
90929	“Error cannot de-mute DAC on analogue board”
140000	“”
140001	“I2C to Clock failed”” or “”I2C initialisation failed”
140100	“”
140101	“I2C to Clock failed”” or “”I2C initialisation failed”
141200	“”
141201	“Progressive Scan Board I2C bus busy”
141211	“Progressive Scan Board I2C FLI2200 bus busy”
141212	“Progressive Scan Board I2C FLI2200 read access time-out”
141213	“Progressive Scan Board I2C FLI2200 no read ac-knowledge”
141214	“Progressive Scan Board I2C FLI2200 read failed”
141215	“Progressive Scan Board I2C FLI2200 write ac-cess time-out”
141216	“Progressive Scan Board I2C FLI2200 no write ac-knowledge”
141217	“Progressive Scan Board I2C FLI2200 write failed”
141218	“Progressive Scan Board I2C FLI2200 failed”
141221	“Progressive Scan Board I2C AD7196 bus busy”
141222	“Progressive Scan Board I2C AD7196 read access time-out”
141223	“Progressive Scan Board I2C AD7196 no read ac-knowledge”
141224	“Progressive Scan Board I2C AD7196 read failed”
141225	“Progressive Scan Board I2C AD7196 write ac-cess time-out”
141226	“Progressive Scan Board I2C AD7196 no write ac-knowledge”
141227	“Progressive Scan Board I2C AD7196 write failed”
141228	“Progressive Scan Board I2C AD7196 failed”
141300	“”

Error	Nr Error String
141301	“Progressive Scan Route Enable failed”
141302	“Generating test image in Hostdecoder failed”
141400	“”
141401	“Progressive Scan Route Disable failed”
141402	“Turning off test image in Hostdecoder failed”
141500	“”
141501	“Progressive Scan Board I2C failed”
141600	“”
141601	“Progressive Scan Board I2C failed”

5. Loop tests

The following loops can be distinguished:

- Loops performed on the digital board only
- User Dealer loops performed on the digital and analogue board
- System loops performed via an external connection: outputs are looped back to the inputs.

5.1 Nucleus 900: Digital Audio Loop

This nucleus tests the audio path through the digital board

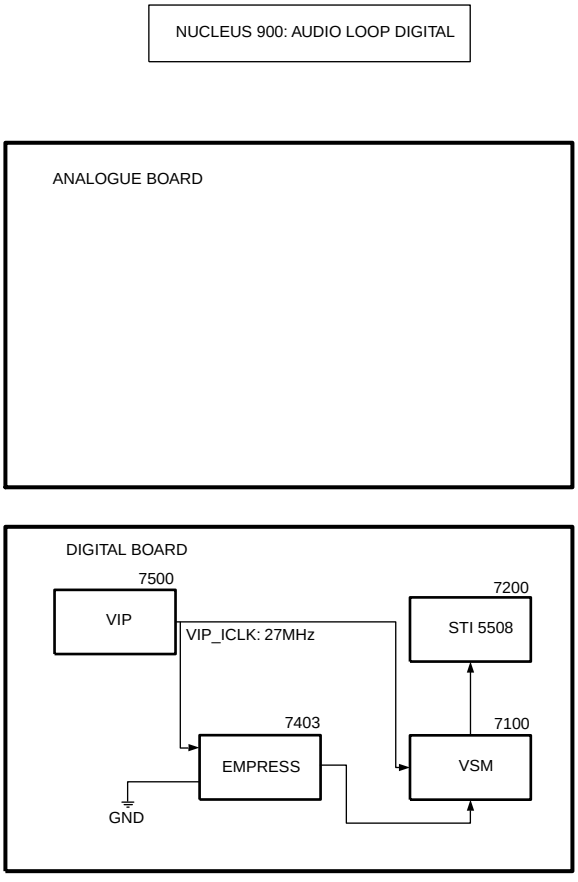


Fig. 9

5.2 Nucleus 901: Audio User Dealer Loop

A PCM audio sine of 12kHz is generated in the Host Decoder for a while and sent to the analogue board. The signal coming from the analogue board is encoded again and sent to the memory of the host decoder for comparison. This nucleus tests the components on the audio signal path:

- Host decoder
- Flex connection between connector 1602 (digital board) and connector 1900 (analogue board)
- DAC
- Op-amp
- Scart switch IC
- ADC
- Audio Encoder
- VIP
- VSM

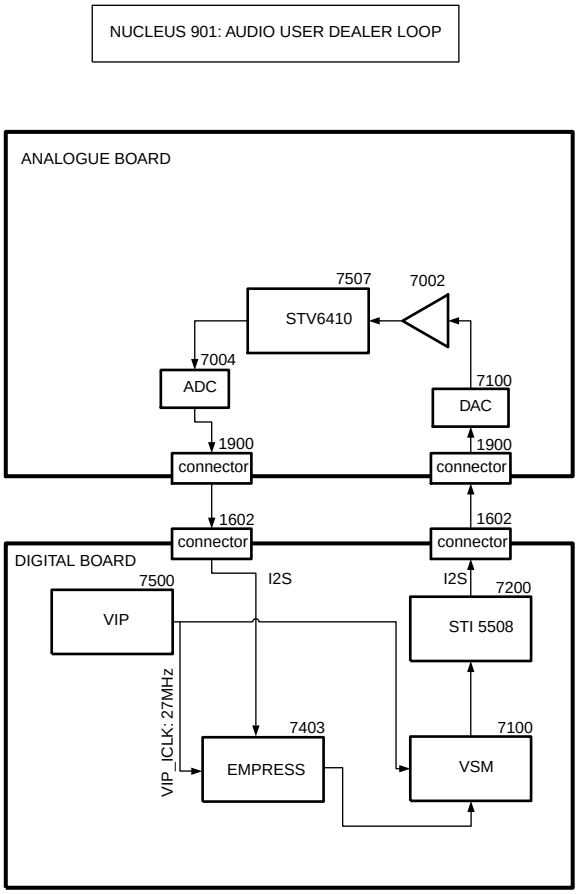


Fig. 10

5.3 Nucleus 902: Digital Video Loop

A colourbar generated in the host decoder is looped through the VIP, Empire, and VSM and checked again in the host decoder. The following components are tested on the video signal path:

- VIP
- Empire
- VSM
- Host decoder

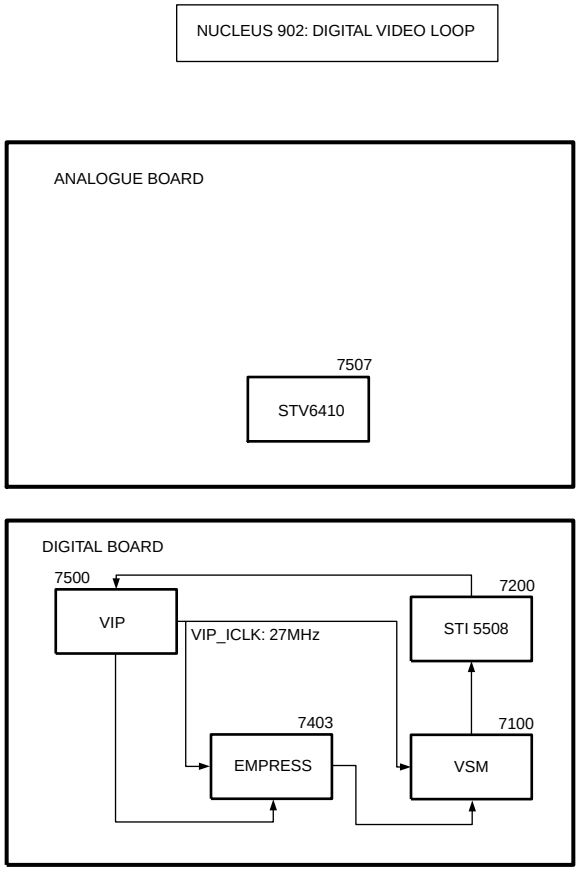


Fig. 11

5.4 Nucleus 903: Digital Video VBI Loop

Nucleus for testing the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

This is done by using the internal test signal source (digital board only)

Remark: this test is only successful if nucleus 121 is carried out first.

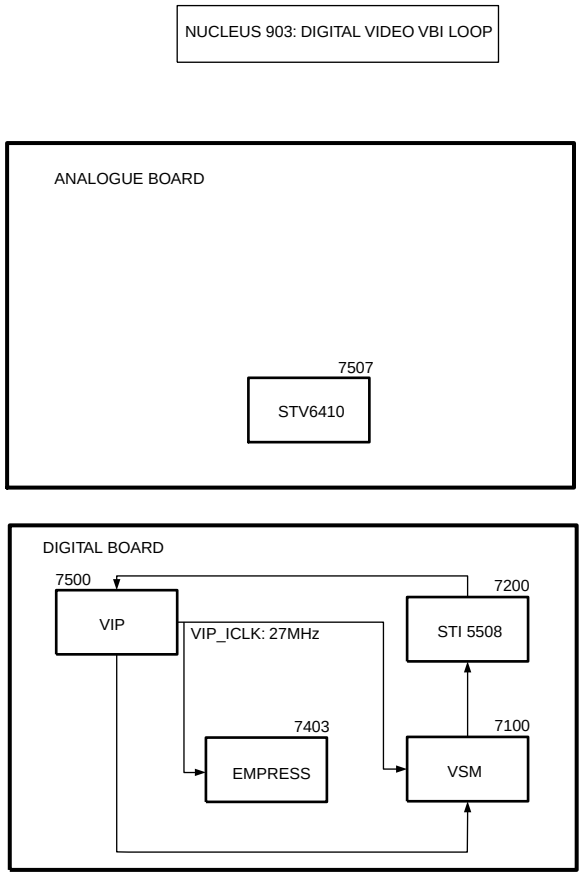


Fig. 12

5.5 Nucleus 904: System Video Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board the video signal will be routed to the SCART (EUROPE) or CINCH (NAFTA). There it will be looped back externally by means of the proper cable.

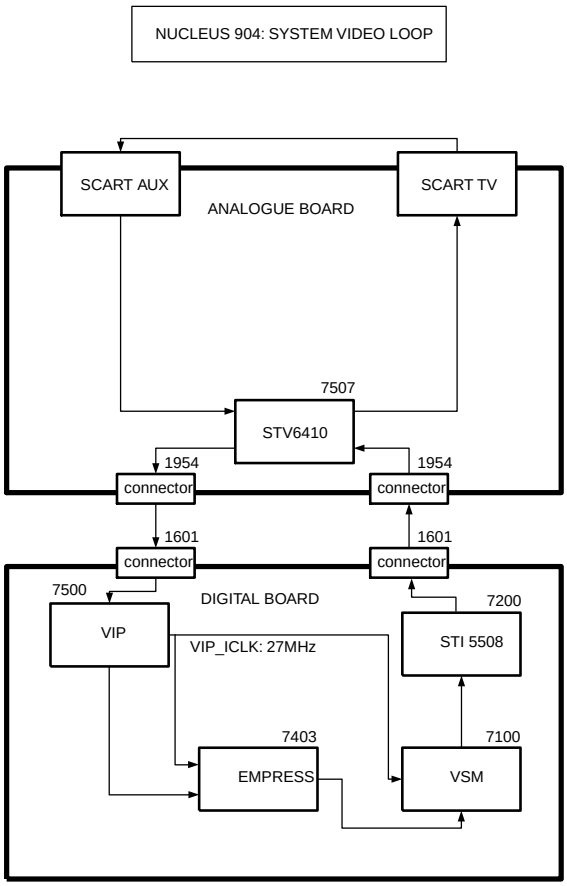


Fig. 13

5.6 Nucleus 905: System Video VBI Loop

This nucleus tests the components on the video signal path:

- The VIP
- The VSM
- The Host Decoder

The video CVBS signal is routed to the output of the analogue board where it will be looped back by means of an external cable.

Remark: this test is only successful if nucleus 121 is carried out first.

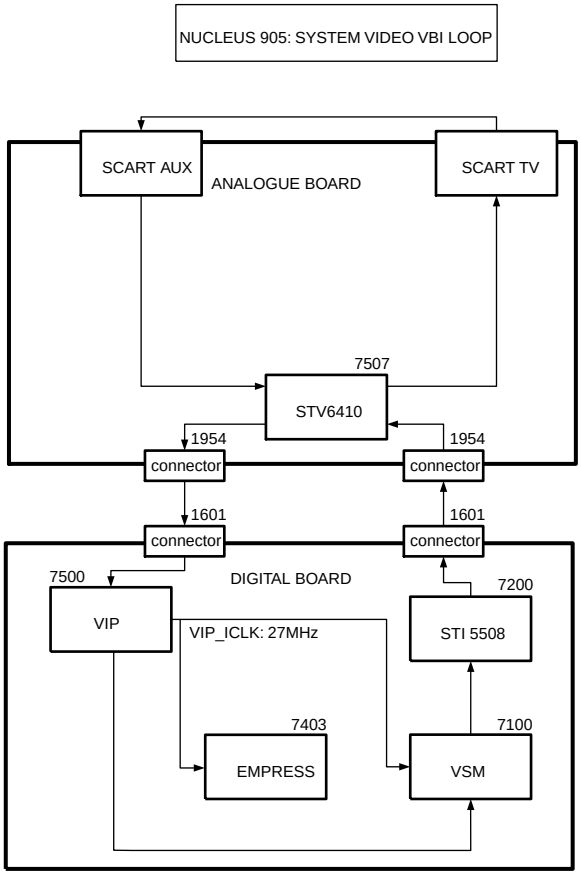


Fig. 14

5.7 Nucleus 906: Video User Dealer Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board, the video signal is internally routed back to the digital board.

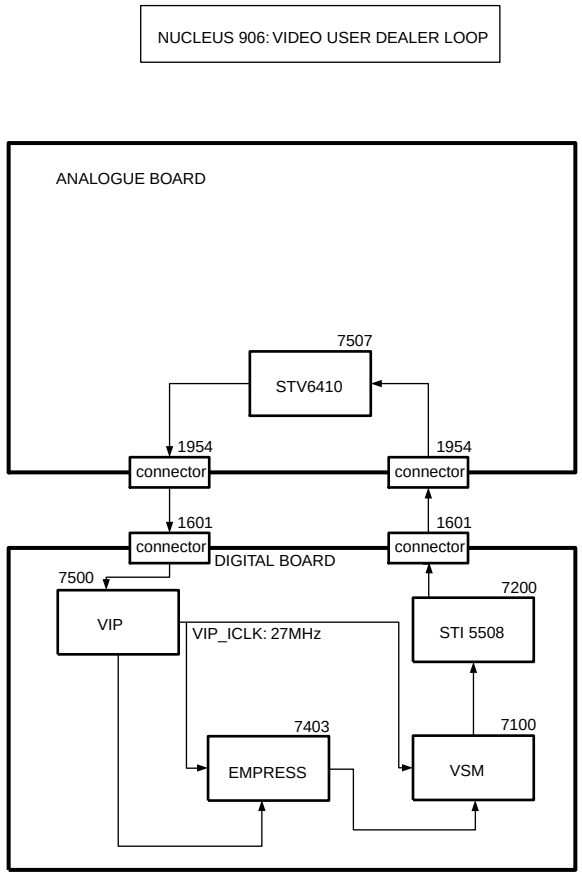


Fig. 15

5.8 Nucleus 907: Video VBI User Dealer Loop

This nucleus tests the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

The signal is routed back internally on the analogue board
Remark: this test is only successful if nucleus 121 is carried out first.

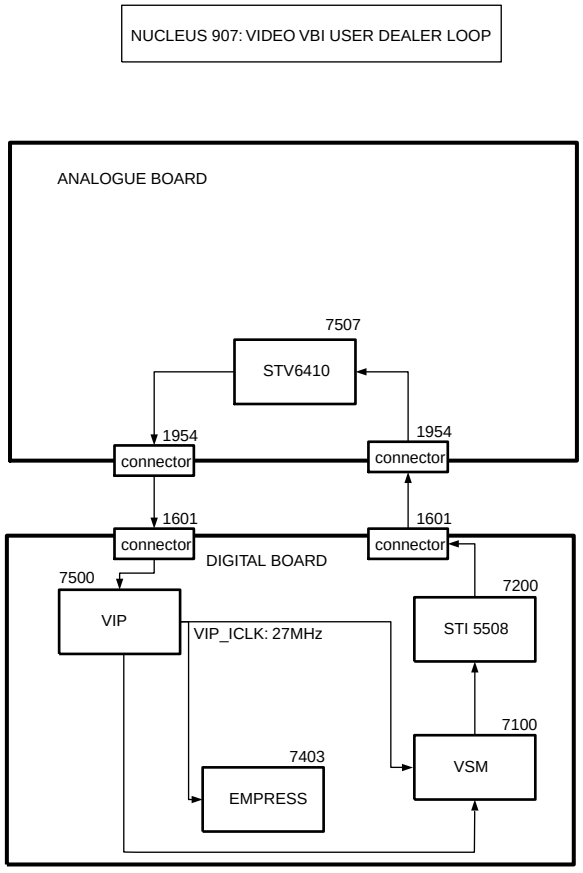


Fig. 16

5.9 Nucleus 908: System Audio Loop Scart (Europe)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board, audio is passed to the SCART connector, where a SCART cable needs to be used to loop back the audio signal to the digital board.

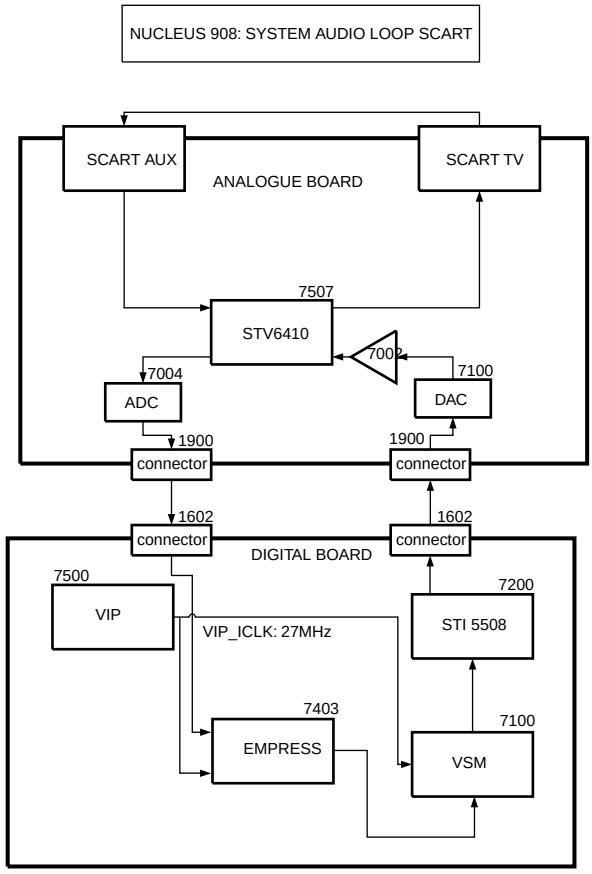


Fig. 17

5.10 Nucleus 909: System Audio Loop CINCH (Nafta)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board the audio is passed to the CINCH connector, where a CINCH cable needs to be used to loop back the audio signal to the digital board.

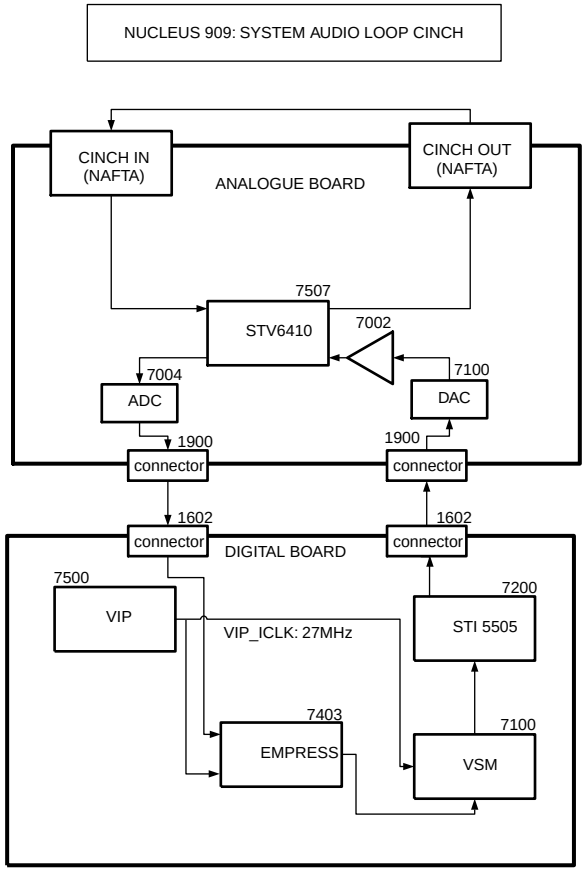


Fig. 18

■ FAULTFINDING TREES

1. General-1

PLAYBACK MODE

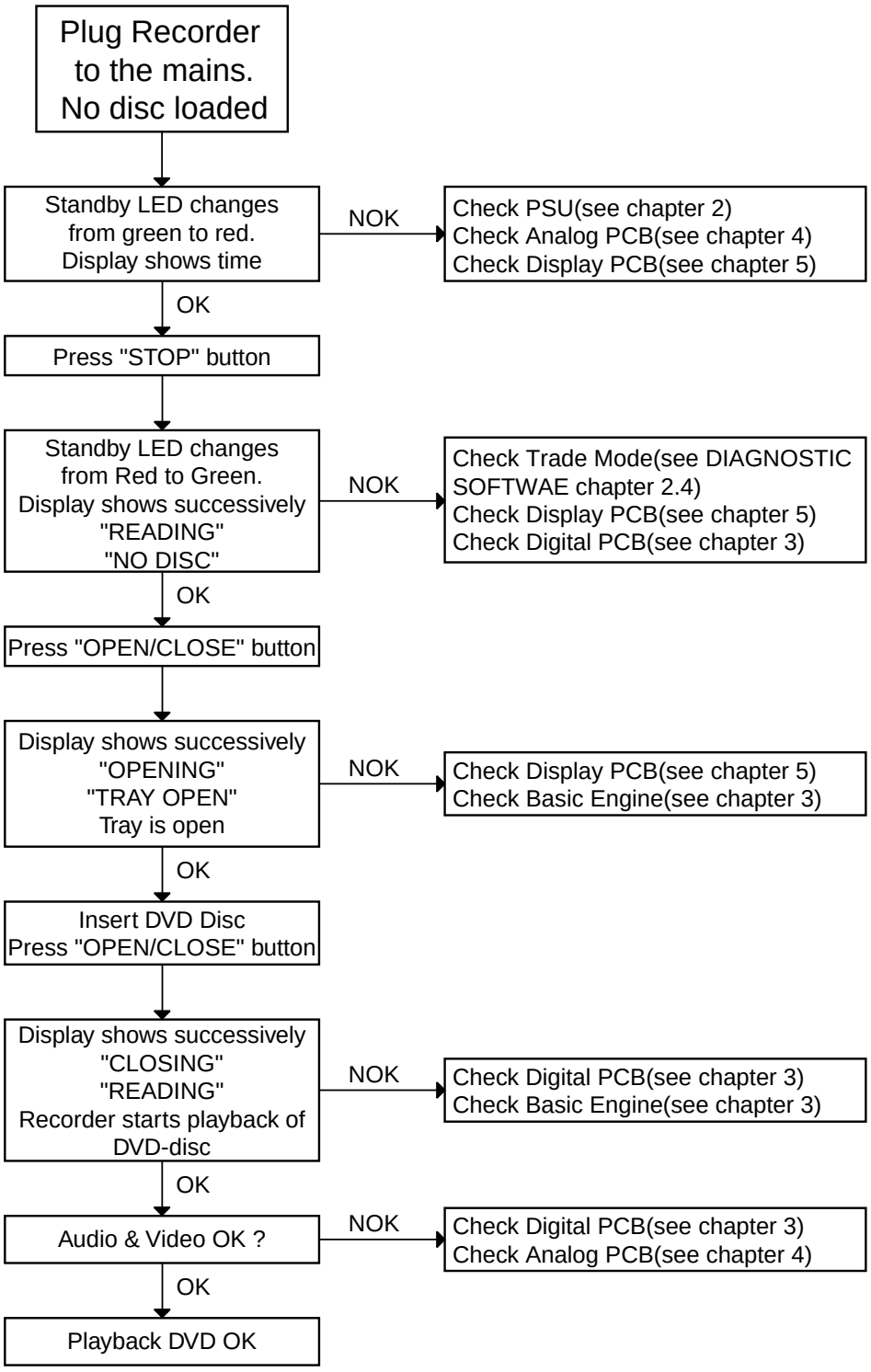

Plug Recorder to the mains. No disc loaded
Standby LED changes from green to red. Display shows time
NOK
Check PSU(see chapter 2)
Check Analog PCB(see chapter 4)
Check Display PCB(see chapter 5)
OK
Press "STOP" button
Standby LED changes from Red to Green. Display shows successively "READING" "NO DISC"
NOK
Check Trade Mode(see DIAGNOSTIC SOFTWAE chapter 2.4)
Check Display PCB(see chapter 5)
Check Digital PCB(see chapter 3)
OK
Press "OPEN/CLOSE" button
Display shows successively "OPENING" "TRAY OPEN" Tray is open
NOK
Check Display PCB(see chapter 5)
Check Basic Engine(see chapter 3)
OK
Insert DVD Disc Press "OPEN/CLOSE" button
Display shows successively "CLOSING" "READING" Recorder starts playback of DVD-disc
NOK
Check Digital PCB(see chapter 3)
Check Basic Engine(see chapter 3)
OK
Audio & Video OK ?
NOK
Check Digital PCB(see chapter 3)
Check Analog PCB(see chapter 4)
OK
Playback DVD OK

Fig. 1

RECORD MODE

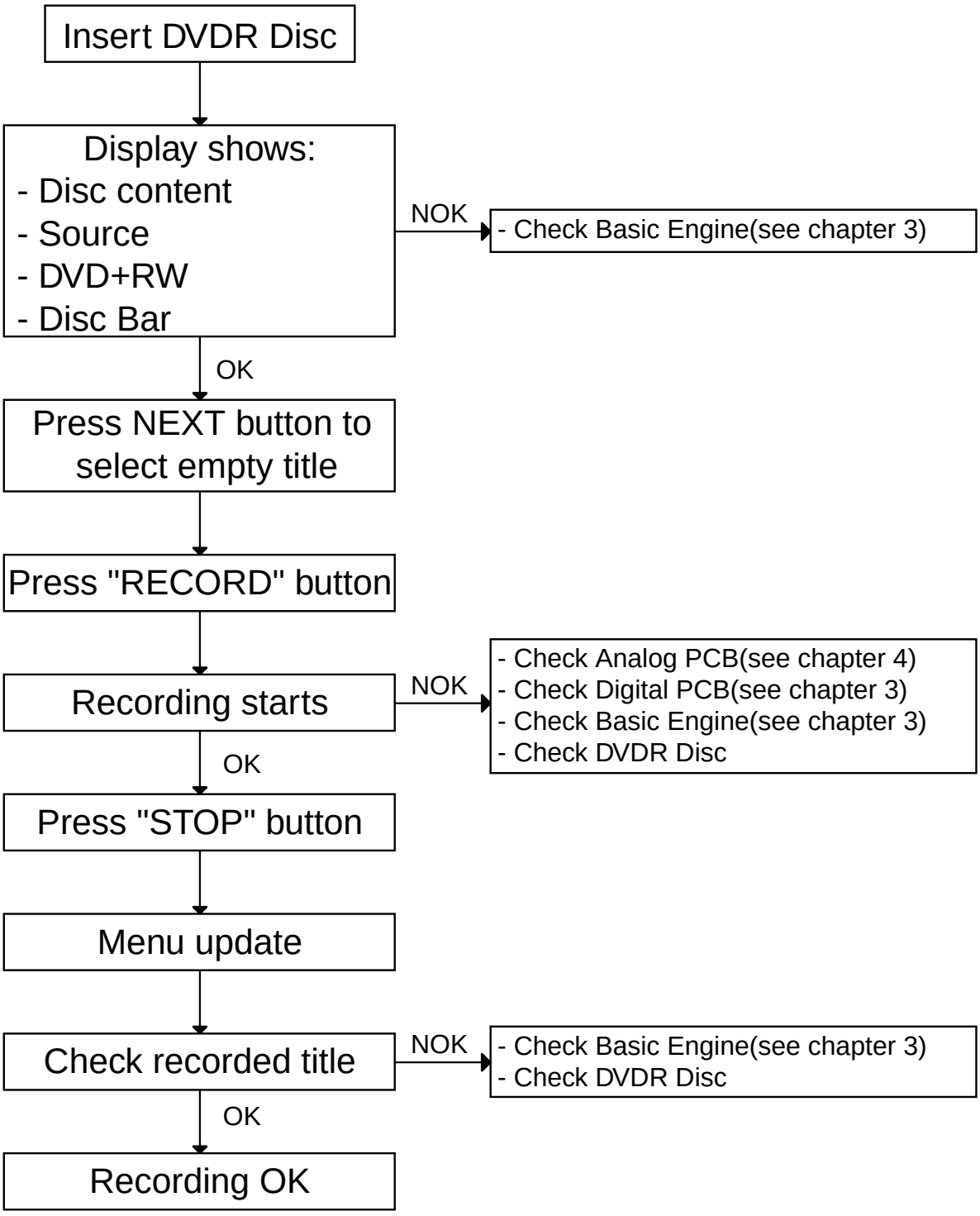


Fig. 2

2. Power Supply

Remove all the connectors from the PSU
Check DC voltages on connector 0205:
+12Vstby, +5V2stby, -5Nstby, -Vgnstby, +33Vstby

None of the voltages are present

Check +12Vreg circuit:
- D6210, C2210, C2212

Check +Vreg circuit:
- D6240, C2240, C2242

Check Prot_3V3 circuit:
- D6215, C2214, C2215,
- R3520, R3521, D6520

Connect PSU to a mains isolated variac. Turn the input voltage up and measure voltage across C2125. Do not exceed max. mains voltage indicated on player. This voltage must be +/- 1.41 x Vin AC.

Check primary circuit:
- F1120, D6151, D6152, D6153, D6154,
- R3120, L5120, L5520, C2125.

If fuse 1120 is defective, always check Q7125, D6145, T7140, Rsense (R3133, R3134, R3135, R3136 and R3137).

Check with an oscilloscope Vds and Vg of Q7125.

Is PSU ticking?

NO

YES

Check power switch circuit:
- Q7125, D6130, D3131, D6132
- D6145, D6146, L5125
- C2136
- R3131, R3132, R3133, R3134
- R3135, R3136, R3137, R3146

Check Control circuit
- T7140, D6141, D6142, L5131,
- C2144, C2145, C2147, C2151
- R3151, R3147, R3148, R3150

Check Regulation circuit
- T7251, Q7200, R3250, R3253
- R3254, R3255, R3256, C2251

Check Overvoltage circuit
- T7142, D6143, D6144,
- R3149, R3144, C2152, C2142

Check Overload circuit
- T7141, T7143, R3145, R3143,
- R3142, C2143.

Check start-up circuit:
- R3125, R3126, R3141, R3132
- Q7125, L5131, R3150, C2146

+12Vstby and +5V2stby are OK.

Check +33Vstby circuit:
- D6200, C2200, R3200, D6201, R3201

Check -5Nstby circuit:
- D6220, C2220, IC7220, C2222, C2221

Check FLYB circuit:
- D6221, T7241, R3220, R3221, R3222, R3223.

Check -Vgnstby circuit:
- D6230, C2230, R3230, D6231, R3233, R3234, C2235.

All voltages are present.

Standby voltages are oke. Check DC voltages on connectors 0207 and 0209.
Connector 0207:
+3V3, +5V, -5V, +12V.
Connector 0209:
+3V3, +12V, +5V, -5V, STBY_ctrl.

If not OK, check supply path of failed supply voltages.

Check if STBY_ctrl is LOW.
- Check standby control path via digital board to analog board.

Check +12V circuit:
must be present for the other voltages
- Q7511, T7512, D6511, D6512,
- R3511, R3513, R3514, L551, C2512.

Check +3V3 circuit:
- Q7520, Q7521, L5520, C2521, F1520,
- R3522, R3523, R3524, R3525, C2520.

Check +5V circuit:
- Q7501, Q7502, L5501, C2502, R3501
- R3502, R3503, R3504, C2540.

Check +3V3E circuit:
- Q7505, Q7506, D6505, L5505, C2506,
- R3505, R3506, R3507, R3508, C2502.

Check -5V circuit:
- Q7515, D6515, L5515, C2515, R3515.

If oke, the power supply seems to be ok. Check the other boards in the player for the cause of the overload.

Fig. 3

3. Digital Board-1

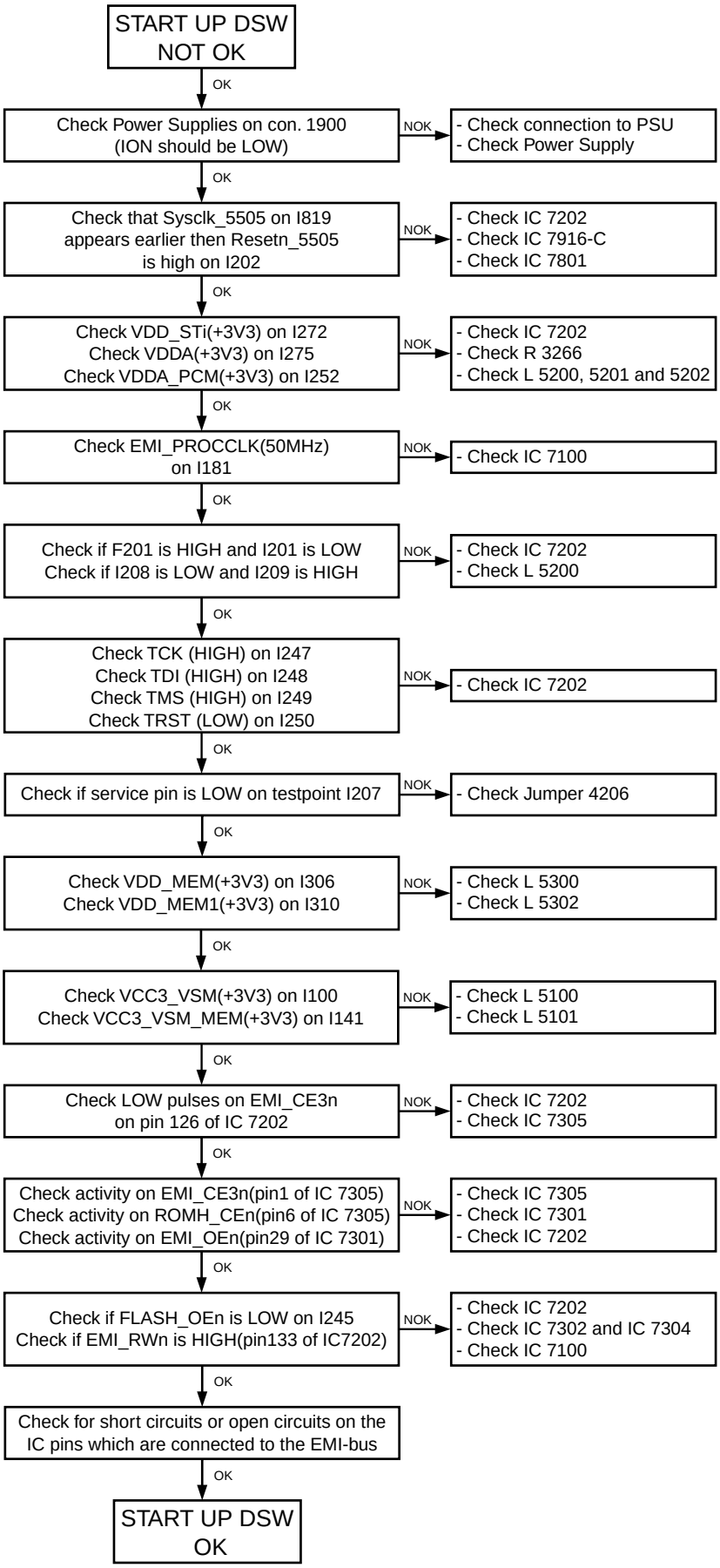

START UP DSW NOT OK
OK
Check Power Supplies on con. 1900 (ION should be LOW)
NOK
- Check connection to PSU
- Check Power Supply
OK
Check that Sysclk_5505 on I819 appears earlier then Resetn_5505 is high on I202
NOK
- Check IC 7202
- Check IC 7916-C
- Check IC 7801
OK
Check VDD_STi(+3V3) on I272
Check VDDA(+3V3) on I275
Check VDDA_PCM(+3V3) on I252
NOK
- Check IC 7202
- Check R 3266
- Check L 5200, 5201 and 5202
OK
Check EMI_PROCCLK(50MHz) on I181
NOK
- Check IC 7100
OK
Check if F201 is HIGH and I201 is LOW
Check if I208 is LOW and I209 is HIGH
NOK
- Check IC 7202
- Check L 5200
OK
Check TCK (HIGH) on I247
Check TDI (HIGH) on I248
Check TMS (HIGH) on I249
Check TRST (LOW) on I250
NOK
- Check IC 7202
OK
Check if service pin is LOW on testpoint I207
NOK
- Check Jumper 4206
OK
Check VDD_MEM(+3V3) on I306
Check VDD_MEM1(+3V3) on I310
NOK
- Check L 5300
- Check L 5302
OK
Check VCC3_VSM(+3V3) on I100
Check VCC3_VSM_MEM(+3V3) on I141
NOK
- Check L 5100
- Check L 5101
OK
Check LOW pulses on EMI_CE3n on pin 126 of IC 7202
NOK
- Check IC 7202
- Check IC 7305
OK
Check activity on EMI_CE3n(pin1 of IC 7305)
Check activity on ROMH_CEn(pin6 of IC 7305)
Check activity on EMI_OEn(pin29 of IC 7301)
NOK
- Check IC 7305
- Check IC 7301
- Check IC 7202
OK
Check if FLASH_OEn is LOW on I245
Check if EMI_RWn is HIGH(pin133 of IC7202)
NOK
- Check IC 7202
- Check IC 7302 and IC 7304
- Check IC 7100
OK
Check for short circuits or open circuits on the IC pins which are connected to the EMI-bus
OK
START UP DSW OK

Fig. 4

3. Digital Board-2

POWER PART CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1 2, 3, 4, 5, 7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

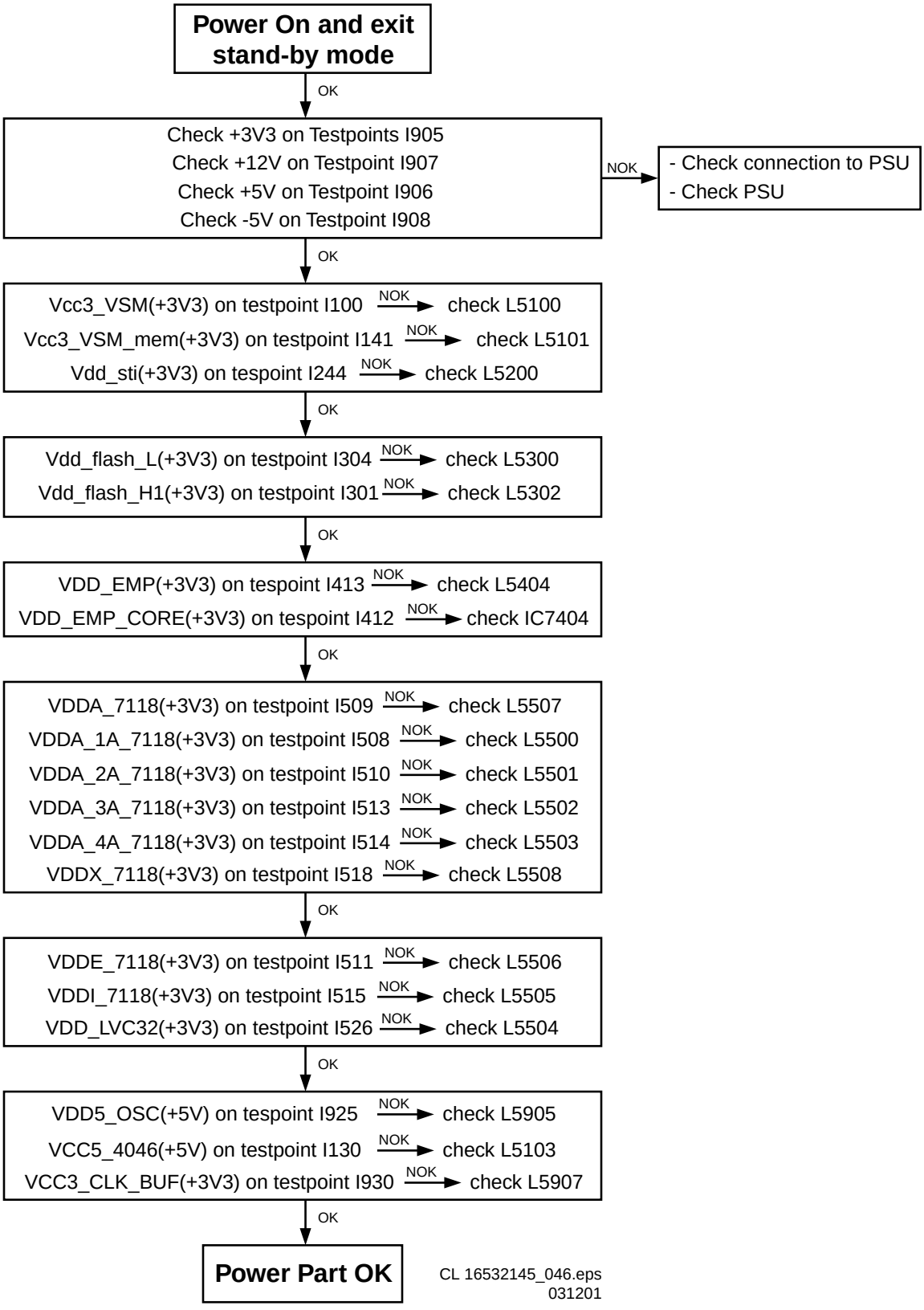

Power On and exit stand-by mode
OK
Check +3V3 on Testpoints I905
Check +12V on Testpoint I907
Check +5V on Testpoint I906
Check -5V on Testpoint I908
NOK
- Check connection to PSU
- Check PSU
OK
Vcc3_VSM(+3V3) on testpoint I100 NOK check L5100
Vcc3_VSM_mem(+3V3) on testpoint I141 NOK check L5101
Vdd_sti(+3V3) on tespoint I244 NOK check L5200
OK
Vdd_flash_L(+3V3) on testpoint I304 NOK check L5300
Vdd_flash_H1(+3V3) on testpoint I301 NOK check L5302
OK
VDD_EMP(+3V3) on tespoint I413 NOK check L5404
VDD_EMP_CORE(+3V3) on tespoint I412 NOK check IC7404
OK
VDDA_7118(+3V3) on testpoint I509 NOK check L5507
VDDA_1A_7118(+3V3) on testpoint I508 NOK check L5500
VDDA_2A_7118(+3V3) on testpoint I510 NOK check L5501
VDDA_3A_7118(+3V3) on testpoint I513 NOK check L5502
VDDA_4A_7118(+3V3) on testpoint I514 NOK check L5503
VDDX_7118(+3V3) on testpoint I518 NOK check L5508
OK
VDDE_7118(+3V3) on testpoint I511 NOK check L5506
VDDI_7118(+3V3) on testpoint I515 NOK check L5505
VDD_LVC32(+3V3) on testpoint I526 NOK check L5504
OK
VDD5_OSC(+5V) on tespoint I925 NOK check L5905
VCC5_4046(+5V) on testpoint I130 NOK check L5103
VCC3_CLK_BUF(+3V3) on testpoint I930 NOK check L5907
OK
Power Part OK
CL 16532145_046.eps
031201

Fig. 5

3. Digital Board-3

RESET & CLOCK CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1,2,7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

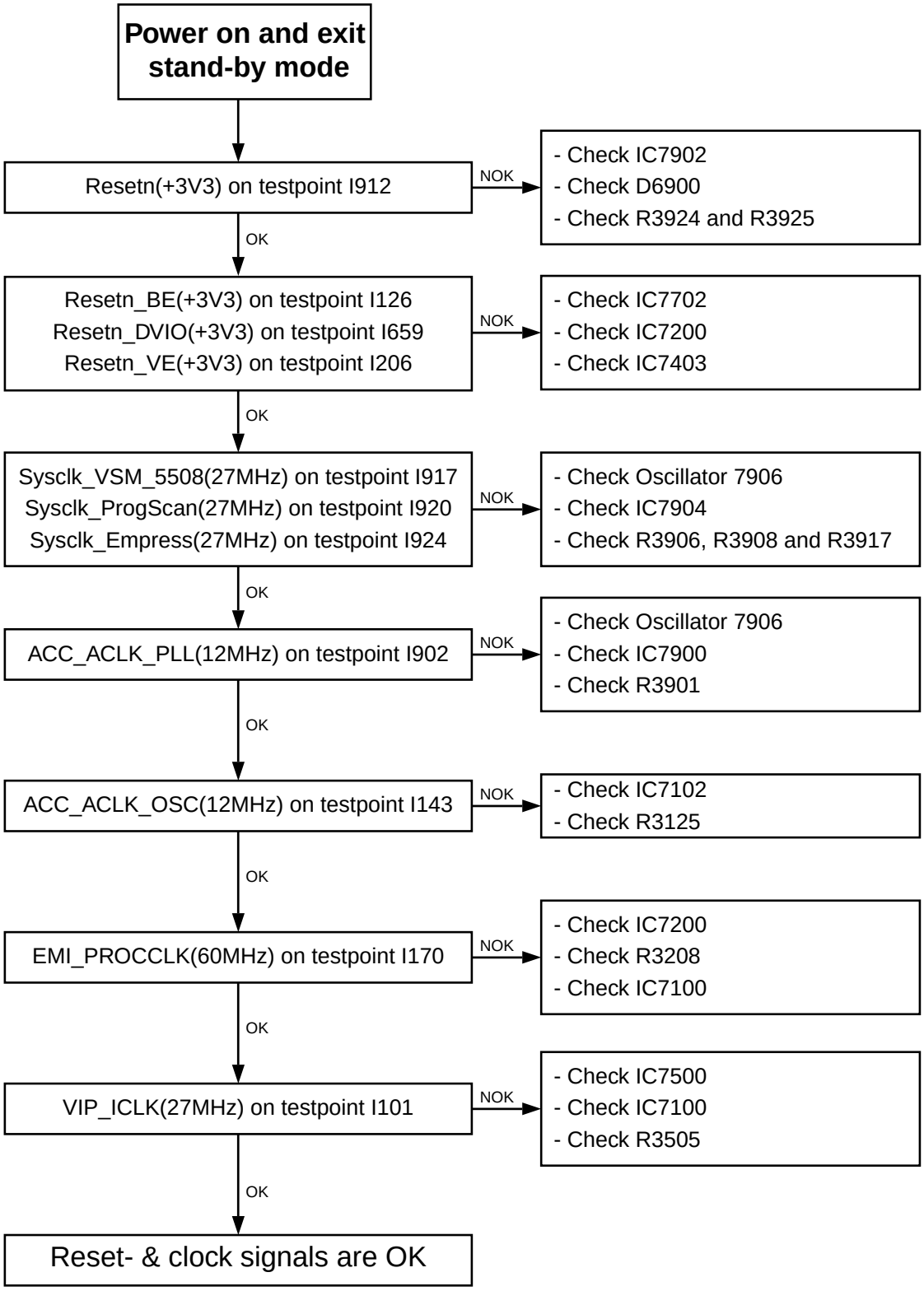


Fig. 6

3. Digital Board-4

DSW MEMORY TESTS

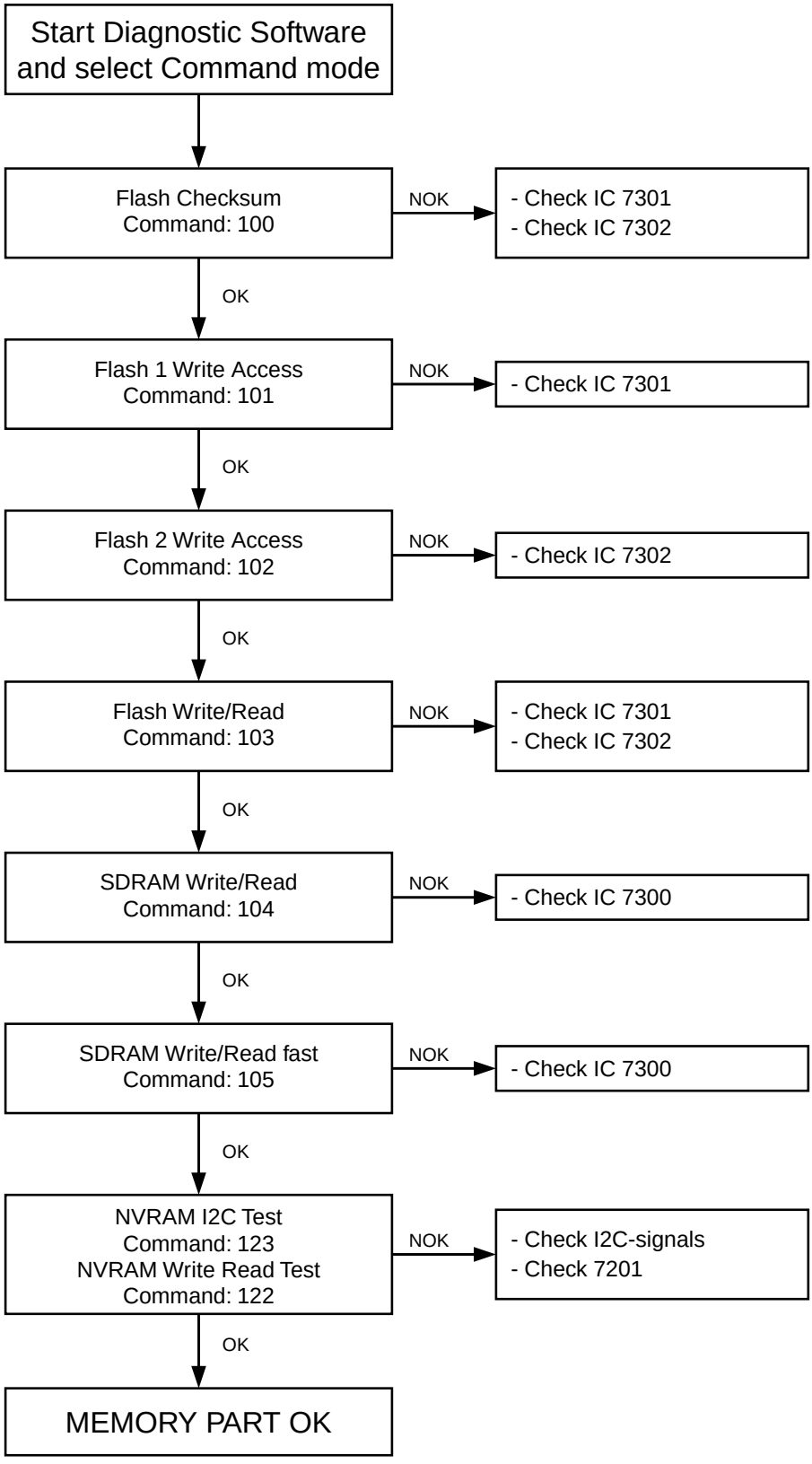


Fig. 7

3. Digital Board-5

DSW VSM TESTS

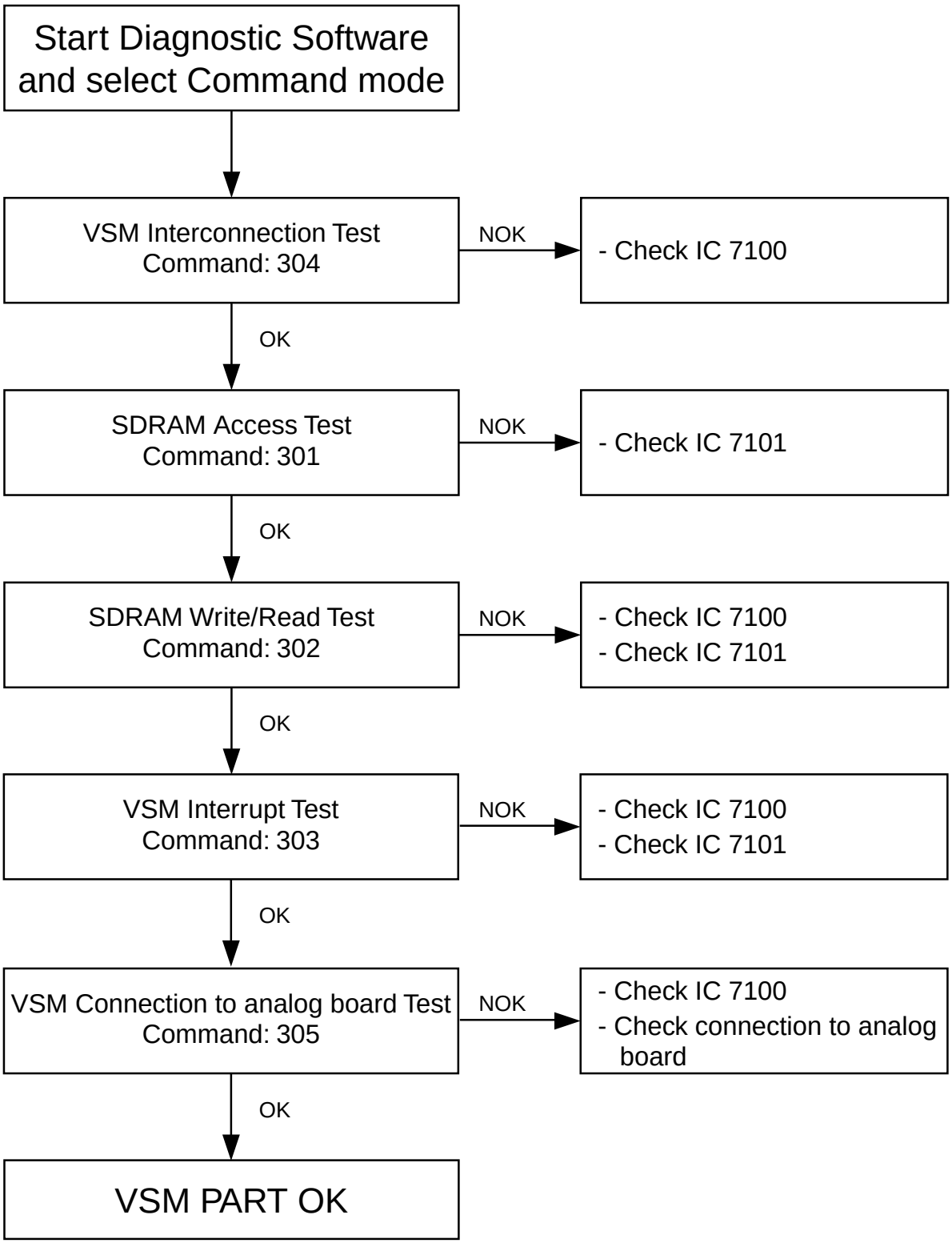


Fig. 8

3. Digital Board-6

DSW AUDIO PART CHECK

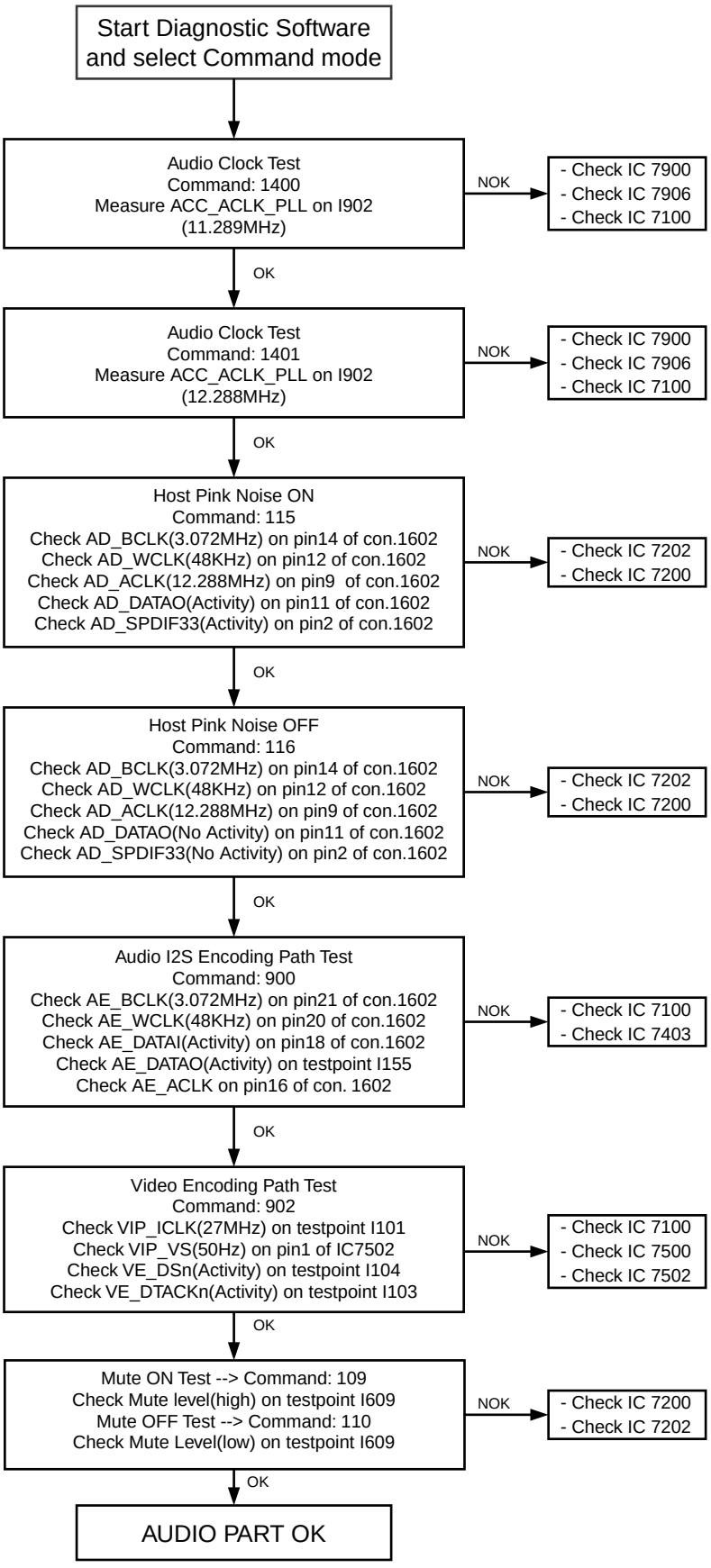


Fig. 9

3. Digital Board-7

DSW VIDEO PART CHECK

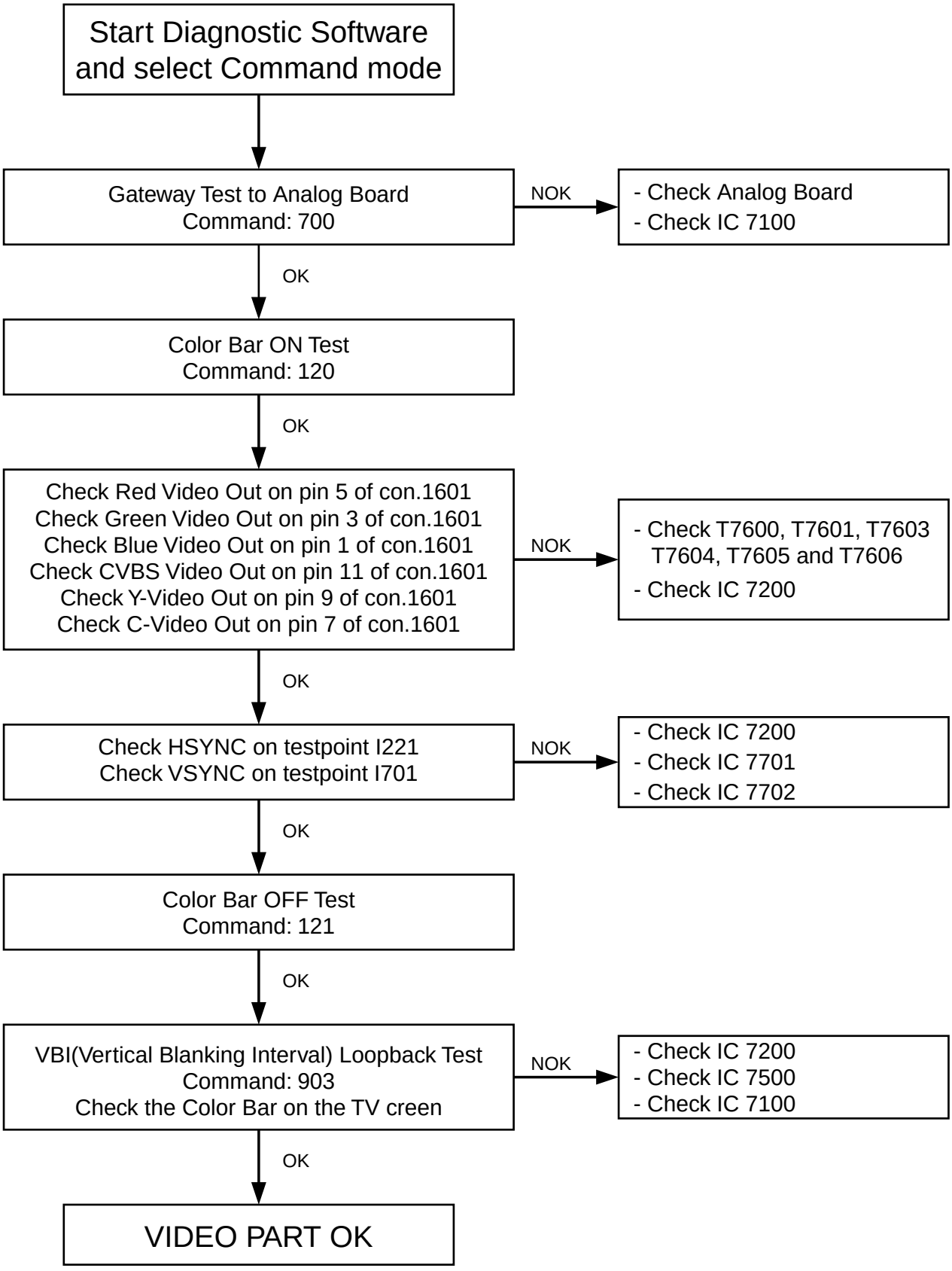

Start Diagnostic Software and select Command mode
Gateway Test to Analog Board Command: 700
NOK
- Check Analog Board
- Check IC 7100
OK
Color Bar ON Test Command: 120
OK
Check Red Video Out on pin 5 of con.1601
Check Green Video Out on pin 3 of con.1601
Check Blue Video Out on pin 1 of con.1601
Check CVBS Video Out on pin 11 of con.1601
Check Y-Video Out on pin 9 of con.1601
Check C-Video Out on pin 7 of con.1601
NOK
- Check T7600, T7601, T7603 T7604, T7605 and T7606
- Check IC 7200
OK
Check HSYNC on testpoint I221
Check VSYNC on testpoint I701
NOK
- Check IC 7200
- Check IC 7701
- Check IC 7702
OK
Color Bar OFF Test Command: 121
OK
VBI(Vertical Blanking Interval) Loopback Test Command: 903
Check the Color Bar on the TV creen
NOK
- Check IC 7200
- Check IC 7500
- Check IC 7100
OK
VIDEO PART OK

Fig. 10

3. Digital Board-8

VIDEO PART CHECK PROGRESSIVE SCAN

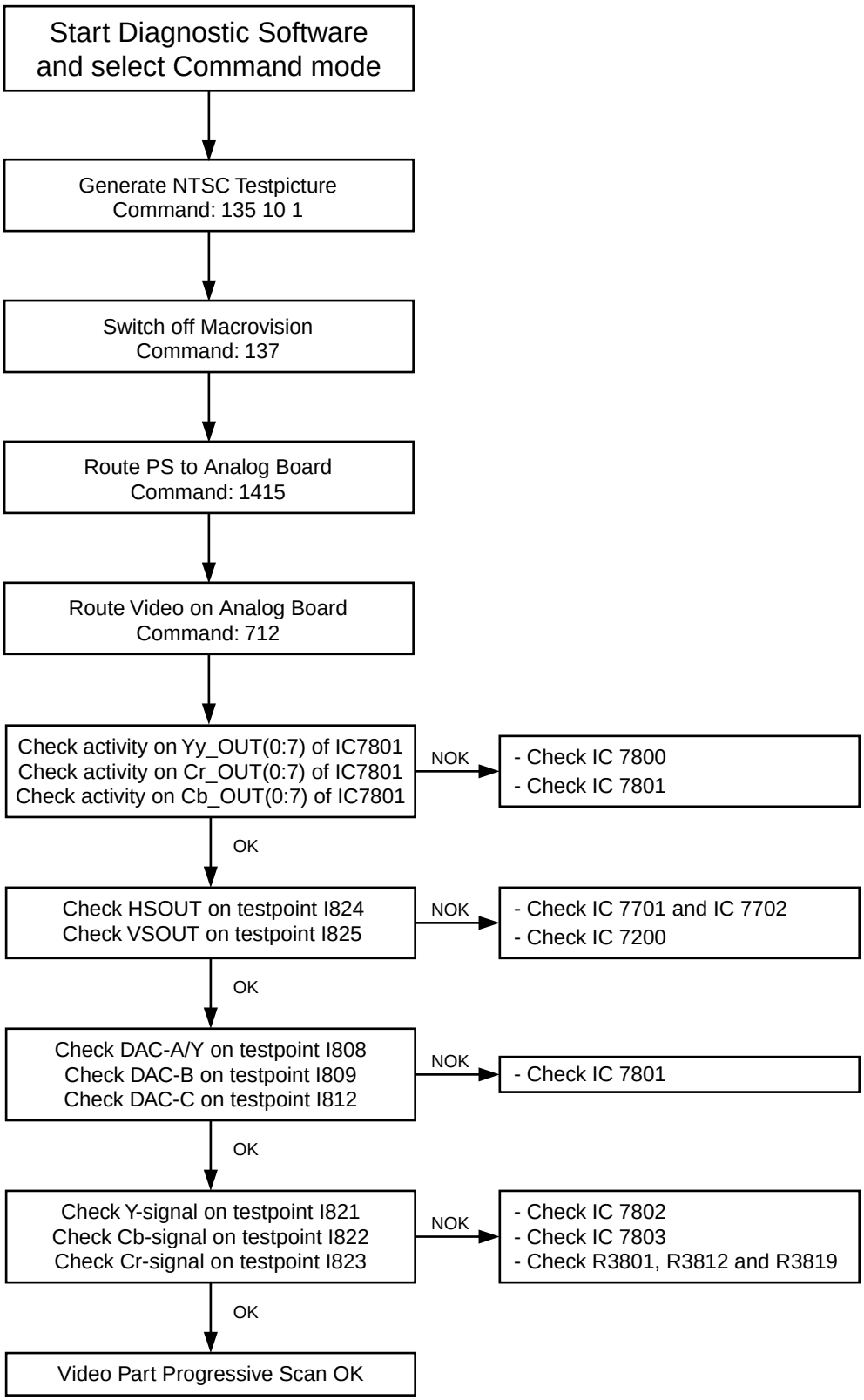

Start Diagnostic Software and select Command mode
Generate NTSC Testpicture Command: 135 10 1
Switch off Macrovision Command: 137
Route PS to Analog Board Command: 1415
Route Video on Analog Board Command: 712
Check activity on Yy_OUT(0:7) of IC7801
Check activity on Cr_OUT(0:7) of IC7801
Check activity on Cb_OUT(0:7) of IC7801
NOK
- Check IC 7800
- Check IC 7801
OK
Check HSOUT on testpoint I824
Check VSOUT on testpoint I825
NOK
- Check IC 7701 and IC 7702
- Check IC 7200
OK
Check DAC-A/Y on testpoint I808
Check DAC-B on testpoint I809
Check DAC-C on testpoint I812
NOK
- Check IC 7801
OK
Check Y-signal on testpoint I821
Check Cb-signal on testpoint I822
Check Cr-signal on testpoint I823
NOK
- Check IC 7802
- Check IC 7803
- Check R3801, R3812 and R3819
OK
Video Part Progressive Scan OK

Fig. 11

3. Digital Board-9

DSW BASIC ENGINE TESTS

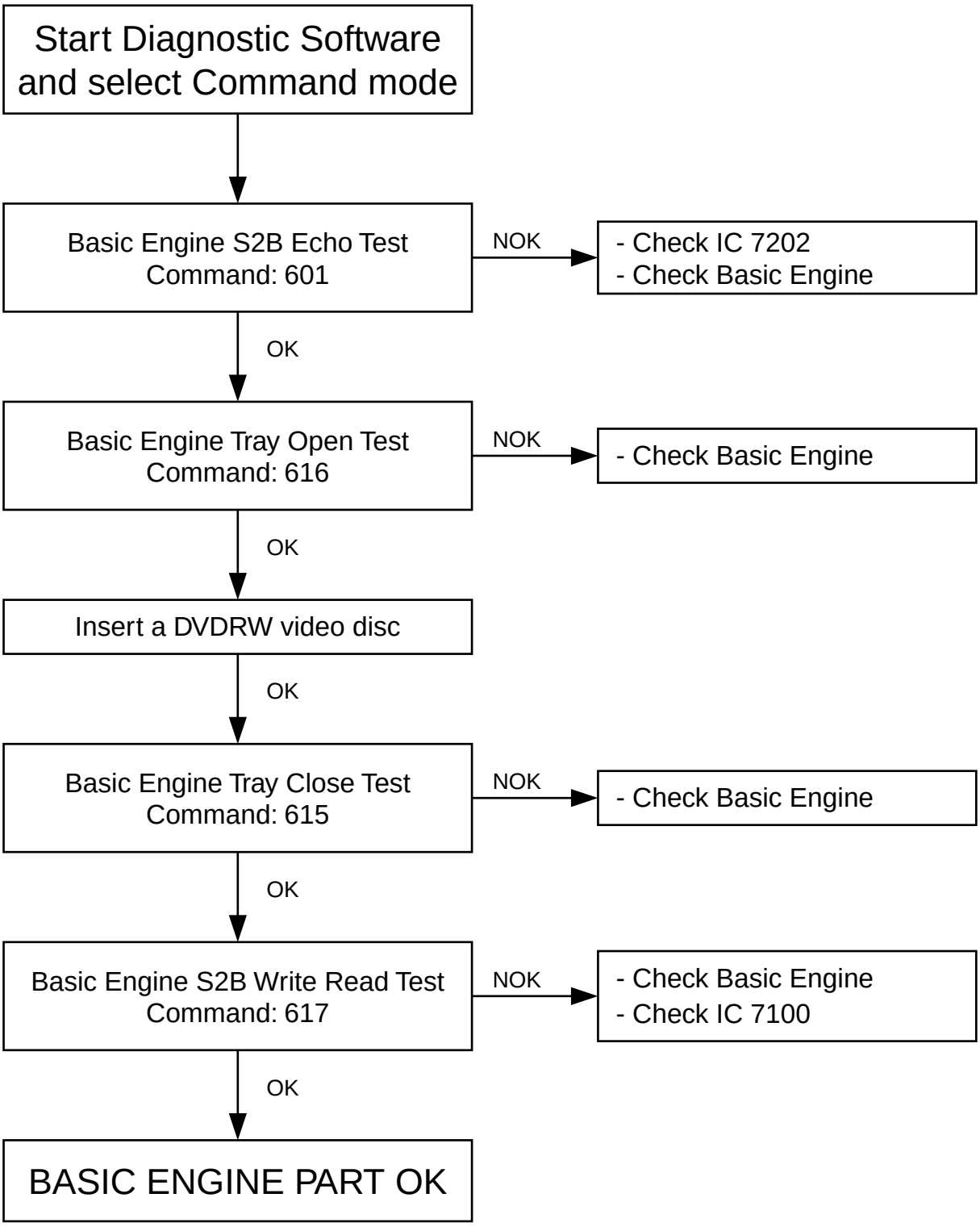
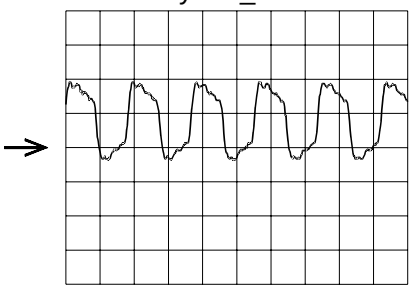


Fig. 12

3. Digital Board-10

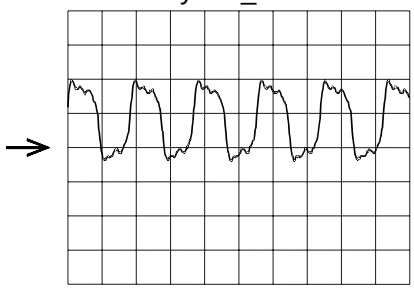
Waveforms Digital Board

Sysclk_VSM



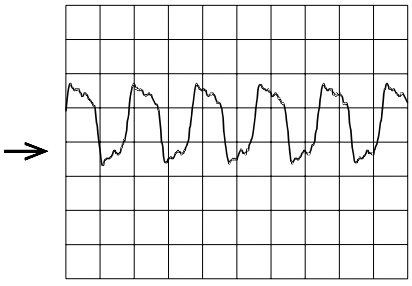
2V / div DC 20ns / div

Sysclk_5505



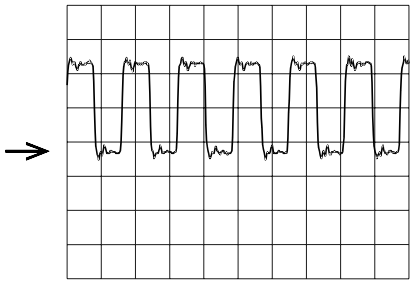
2V / div DC 20ns / div

27M_clk_PS



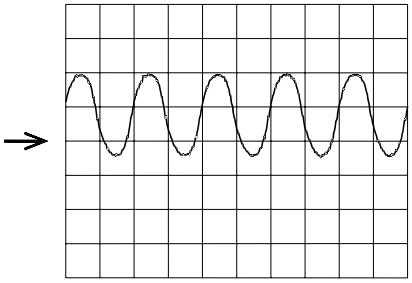
2V / div DC 20ns / div

acc_aclk_pll



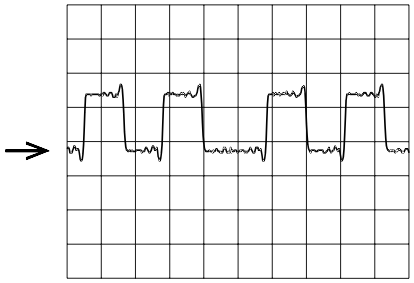
2V / div DC 50ns / div

EMI_PROCCLK



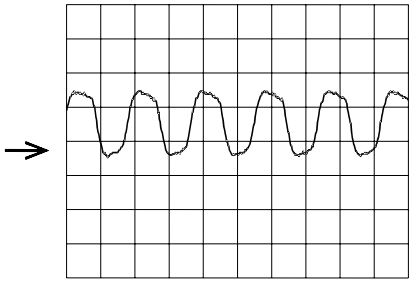
2V / div DC 10ns / div

DSP_clk



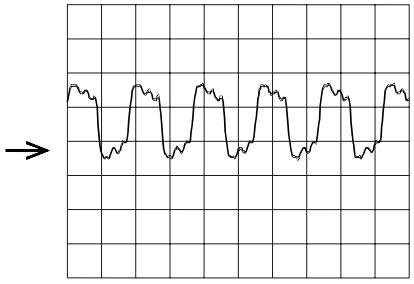
2V / div DC 10ms / div

VIP_ICLK



2V / div DC 20ns / div

VSM_M_CLK



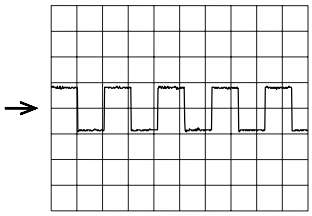
2V / div DC 20ns / div

Fig. 13

3. Digital Board-11

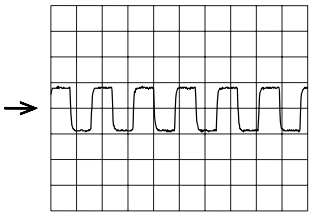
Waveforms Digital Board

AD_WCLK; AE_WCLK



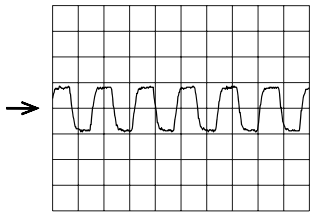
2V / div AC 10us / div

AD_BCLK; AE_BCLK



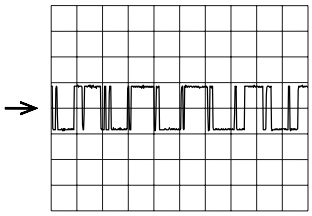
2V / div AC 200ns / div

AD_ACLK



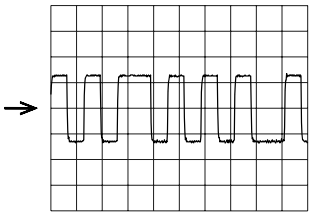
2V / div AC 50ns / div

AD_DATAO; AE_DATAO; AE_DATAI



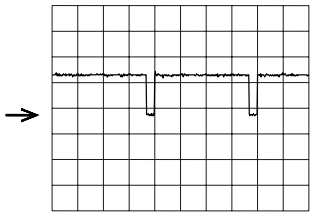
2V / div AC 5us / div

AD_SPDIF



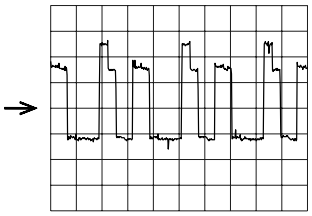
2V / div AC 250ns / div

I401 VIP_VS



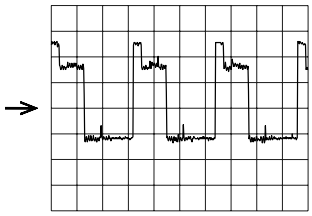
2V / div DC 5ms / div

R_OUT



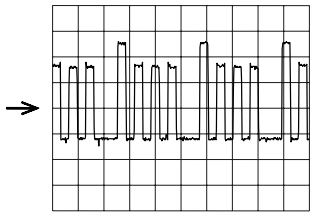
200mV / div AC 20us / div

G_OUT



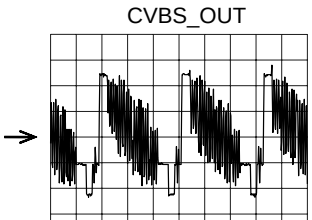
200mV / div AC 20us / div

B_OUT



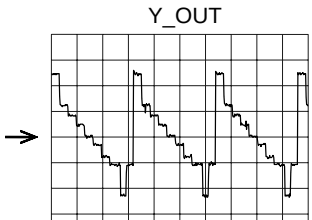
200mV / div AC 20us / div

CVBS_OUT



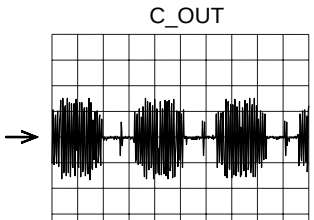
200mV / div AC 20us / div

Y_OUT



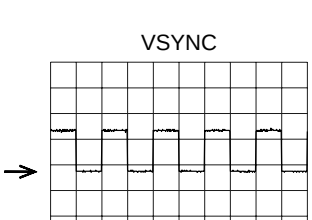
200mV / div AC 20us / div

C_OUT



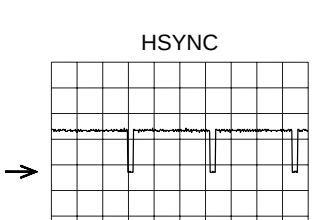
200mV / div AC 20us / div

VSYNC



2V / div DC 20ms / div

HSYNC



2V / div DC 20ms / div

Fig. 14

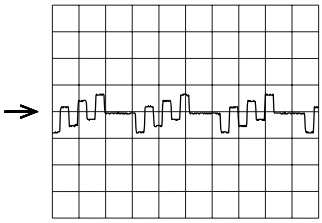
3. Digital Board-12

Waveforms Digital Board

DAC-B

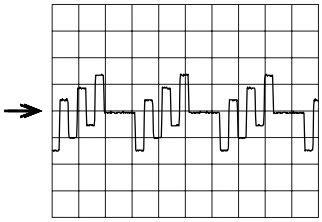
500mV / div AC 10us / div

DAC-A/Y



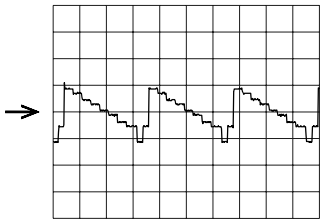
500mV / div AC 10us / div

Cr-signal



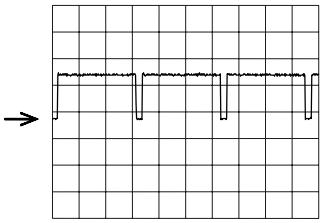
500mV / div AC 10us / div

DAC-C



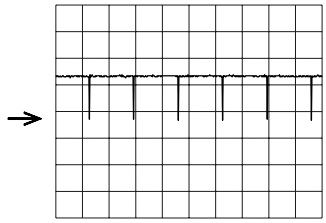
500mV / div AC 10us / div

HS_IN



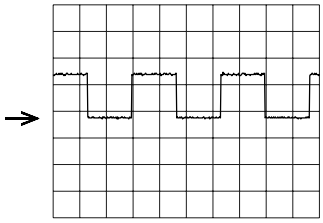
2V / div DC 20us / div

VSOUT



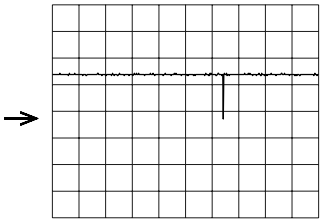
2V / div DC 10ms / div

FRAME_IN



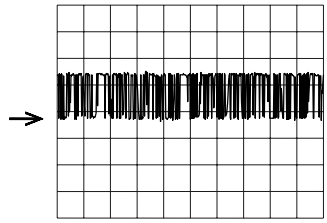
2V / div DC 10ms / div

VS_IN



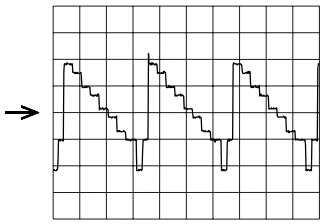
2V / div DC 10ms / div

YUV_IN



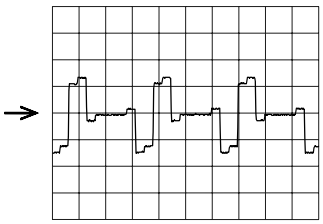
2V / div DC 10ms / div

Y-signal



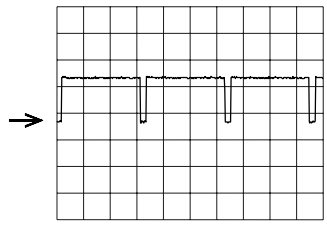
500mV / div AC 10us / div

Cb-signal



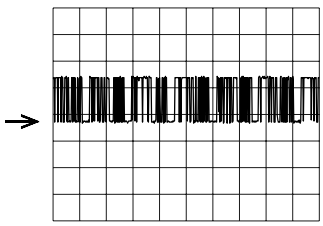
500mV / div AC 10us / div

HSOUT



2V / div DC 10us / div

Y_OUT; Cr_OUT; Cb_OUT



2V / div DC 20us /div

Fig. 15

Measurement Point Overview for A, B, G models -1

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F800			F_MODE	Fact. Mode	Condition	AIO1	AIO1	C10
F3201			12V	12 V Supply	PS IN	1932 1	PS	C1
F3202			5V	5 V Supply	PS IN	1932 2	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204			VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205			33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GNDA	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001			GNDD	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900			5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902			IReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	B6
F8105			SDA	IIC1	IIC IO	1981 6	AIO1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AIO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AIO1	A9
F8104			IPOR1	IPOR to DC	DC OUT	1981 5	AIO1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110			5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC IN	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC IN	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC IN	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC IN	1982 5	AIO1	H13
F8108			INT	TO DC	DC IN	1981 9	AIO1	F13
F8109			RC	TO DC	DC IN	1981 10	AIO1	F13
F8201			IRESET_DIG	TO DIGI	DC IN	1982 1	AIO1	H13
F513			GNDA	SC1 GND A	DC IN	1950 4A	IO1	E14
F517			ARIn_SC1	SC1 A R IN	NF IN	1950 2A	IO1	E13
F519			ALIn_SC1	SC1 A L IN	NF IN	1950 6A	IO1	E14
F534			YCVBSIN_SC1	SC1 Y IN	V IN	1950 20A	IO1	I13
F525			GNDV	SC1 GND V	GND	1950 21A	IO1	H14
F5001			AROut_SC2	SC2 A R Out	NF Out	1950 1B	IO4	C9
F5003			ALOutSC2	SC2 A L Out	NF Out	1950 3B	IO4	C9
F5004			GNDA	SC2 GND A	GND	1950 4B	IO4	C9
F5019			YCVBSOut_SC2	SC2 Y Out	V Out	1950 19B	IO4	C9
F5021			GNDV	SC2 GND V	GND	1950 21B	IO4	C9
F516			AROut_SC1	SC1 A R Out	NF Out	1950 1A	IO1	E14
F518			ALOutSC1	SC1 A L Out	NF Out	1950 3A	IO1	E14
F531			YCVBSOut_SC1	SC1 Y Out	V Out	1950 19A	IO1	G13

Measurement Point Overview for A, B, G models -2

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F5002			ARIn_SC2	SC2 A R IN	NF IN	1950 2B	IO4	C9
F5006			ALIn_SC2	SC2 A L IN	NF IN	1950 6B	IO4	C9
F5020			YCVBSIN_SC2	SC2 Y IN	Sin IN	1950 20B	IO4	F9
F536			BC_SC1	SC1 BC	Sin Out*	1950 7A	IO1	E13
F521			8_SC1	SC1 Pin 8	DC Out	1950 8A	IO1	F13
F515			P50_SC1	SC1 P50	DC Out	1950 10A	IO1	F14
F524			Gout_SC1	SC1 G Out	Sin Out	1950 11A	IO1	F13
F527			RCOut_SC1	SC1 RC Out	Sin Out	1950 15A	IO1	G14
F530			FBOut_SC1	SC1 FB Out	DC Out	1950 16A	IO1	H13
F5007			BC_SC2	SC2 B IN C Out	Sin In*	1950 7B	IO4	D9
F5008			8_SC2	SC2 Pin 8	DC Out	1950 8B	IO4	D9
F5011			Gin_SC2	SC2 G In	Sin In	1950 11B	IO4	D9
F5015			RCin_SC2	SC2 RC In	Sin In	1950 15B	IO4	E9
F5016			FBin_SC2	SC2 FB In	DC In	1950 16B	IO4	E9
F5401			A_V	A_V to DIGI	Sin Out	1954 01	IO1	I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1	I4
F5403			A_U	A_U to DIGI	Sin Out	1954 03	IO1	I4
F5405			A_Y	A_Y to DIGI	V Out	1954 05	IO1	I4
F5407			A_C	A_C to DIGI	Sin Out	1954 07	IO1	I4
F5409			A_YCVBS	AYCVBS to DIGI	V Out	1954 09	IO1	I4
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	IO1	I5
F5414			D_Y	D_Y f. DIGI	V In	1954 14	IO1	I5
F5416			D_C	D_C f. DIGI	Sin In	1954 16	IO1	I5
F5418			D_R	D_T f. DIGI	Sin In	1954 18	IO1	I6
F5420			D_G	D_G f. DIGI	Sin In	1954 20	IO1	I6
F5422			D_B	D_B f. DIGI	Sin In	1954 22	IO1	I6
F5301			AFCRI	A R from FC	NF In	1953 1	IO1	I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1	I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1	I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1	I2
F5309			YFIN	Y from FC	V In	1953 9	IO1	I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC	D2
F0005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F331			RCALOut	A L Rear Cinch Out	NF Out	1958 4B	IO3	E9
F334			RCAROut	A R Rear Cinch Out	NF Out	1958 5B	IO3	E9
F336			RCVBSOut	V Rear Cinch Out	V Out	1959 1B	IO3	C9

Fig. 16

DRX-1

Measurement Point Overview for A, B, G models -3

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F5101			ARCRI	A L Rear Cinch In	NF In	1958 1A	IO2	D2
F5103			ARCLI	A R Rear Cinch In	NF In	1958 2A	IO2	E2
F5202			RCVBSIn	V Rear Cinch In	V In	1959 2A	IO2	C2
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	IO2	B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	IO2	B2
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND	1960 2	AP	D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700			IF	IF Out	DC Out	1705 11	TU	C3
F701			IF In	IF In	Sin In	1705 11	TU	C3
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F703			GNDFV	GND FV	GND	1700 3	TU	B6
F704			40.4	40.4 Trap	Sin Out	1700 1	TU	B5
F705			AGC	AGC	DC Out	3701	TU	A4
F812			SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1	F6
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985 1	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	I13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	I13
F8210			GNDD	GNDD	GNDD	1982 10	AIO1	I13

Fig. 17

Remark:
Indicator * means more than one signal type

Measurement Point Overview for U model -1

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F800			F_MODE	Fact. Mode	Condition	AIO1	AIO1	C10
F3201			12V	12 V Supply	PS IN	1932 1	PS	C1
F3202			5V	5 V Supply	PS IN	1932 2	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204			VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205			33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GNDA	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001			GNDD	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900			5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902			IReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	B6
F8105			SDA	IIC1	IIC IO	1981 6	AIO1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AIO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AIO1	A9
F8104			IPOR1	IPOR to DC	DC OUT	1981 5	AIO1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110			5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC_In	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC_In	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC_In	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC_In	1982 5	AIO1	H13
F8108			INT	TO DC	DC_In	1981 9	AIO1	F13
F8109			RC	TO DC	DC_In	1981 10	AIO1	F13
F8201			IRESET_DIG	TO DIGI	DC_In	1982 1	AIO1	H13
F5103			ARIn_2	A R IN 2	NF IN	1958 3A	IO3	E13
F5101			ALIn_2	A L IN 2	NF IN	1958 1A	IO3	E14
F5906			GNDV	GND V	GND	1957 6A	IO1	H12
F5806			GNDV	GND V	GND	1956 6A	IO1	I8
F510			ARout_1	A R Out 1	NF Out	1959 5B	IO1	E13
F509			ALout_1	A L Out 1	NF Out	1959 4B	IO1	D13
F5201			RCVBSOut2	SC1 Y Out	V Out	1997 1B	IO3	A8
F5105			ARIn_1	A R IN 1	NF IN	1959 1A	IO2	E2
F5104			ALIn_1	A L IN 1	NF IN	1959 4A	IO2	E2
F5202			RCVBSIn	Y IN	Sin IN	1997 2A	IO2	C2
F5905			Y_OUT	Y Out	Sin Out*	1957 5A	IO1	I12
F5801			U_IN	U IN	Sin In*	1956 1B	IO1	I10
F5805			Y_IN	Y IN	Sin In	1956 5A	IO1	I9
F5802			V_IN	V IN	Sin In	1956 2B	IO1	I10

Measurement Point Overview for U model -2

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F5401			A_V	A_V to DIGI	Sin Out	1954 01	IO1	I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1	I4
F5403			A_U	A_U to DIGI	Sin Out	1954 03	IO1	I4
F5405			A_Y	A_Y to DIGI	V Out	1954 05	IO1	I4
F5407			A_C	A_C to DIGI	Sin Out	1954 07	IO1	I4
F5409			A_YCVBS	AYCVBS to DIGI	V Out	1954 09	IO1	I4
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	IO1	I5
F5414			D_Y	D_Y f. DIGI	V In	1954 14	IO1	I5
F5416			D_C	D_C f. DIGI	Sin In	1954 16	IO1	I5
F5418			D_R	D_T f. DIGI	Sin In	1954 18	IO1	I6
F5420			D_G	D_G f. DIGI	Sin In	1954 20	IO1	I6
F5422			D_B	D_B f. DIGI	Sin In	1954 22	IO1	I6
F5301			AFCRI	A R from FC	NF In	1953 1	IO1	I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1	I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1	I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1	I2
F5309			YFIN	Y from FC	V In	1953 9	IO1	I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC	D2
F0005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F513			ALOut_2	A L Rear Out 2	NF Out	1958 4B	IO1	B13
F512			AROut_2	A R Rear Out 2	NF Out	1958 5B	IO1	C13
F5205			RCVBSOut1	V Rear Cinch Out1	V Out	1997 5C	IO3	A8
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	IO2	B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	IO2	B2
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND	1960 2	AP	D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700			IF	IF Out	DC Out	1705 11	TU	C3
F701			IF In	IF In	Sin In	1705 11	TU	C3
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F703			GNDFV	GND FV	GND	1700 3	TU	B6
F705			AGC	AGC	DC Out	3701	TU	A4
F812			SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1	F6
F330			RC IN	Remote Control In	DC Out	1993 2	IO3	E2

Fig. 18

Measurement Point Overview for U model -3

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Schematics Coord.
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	I13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	I13
F8210			GNDD	GNDD	GNDD	1982 10	AIO1	I13

Remark:
Indicator * means more than one signal type

DRX-1

4. Analog Board-4

Power Part Check

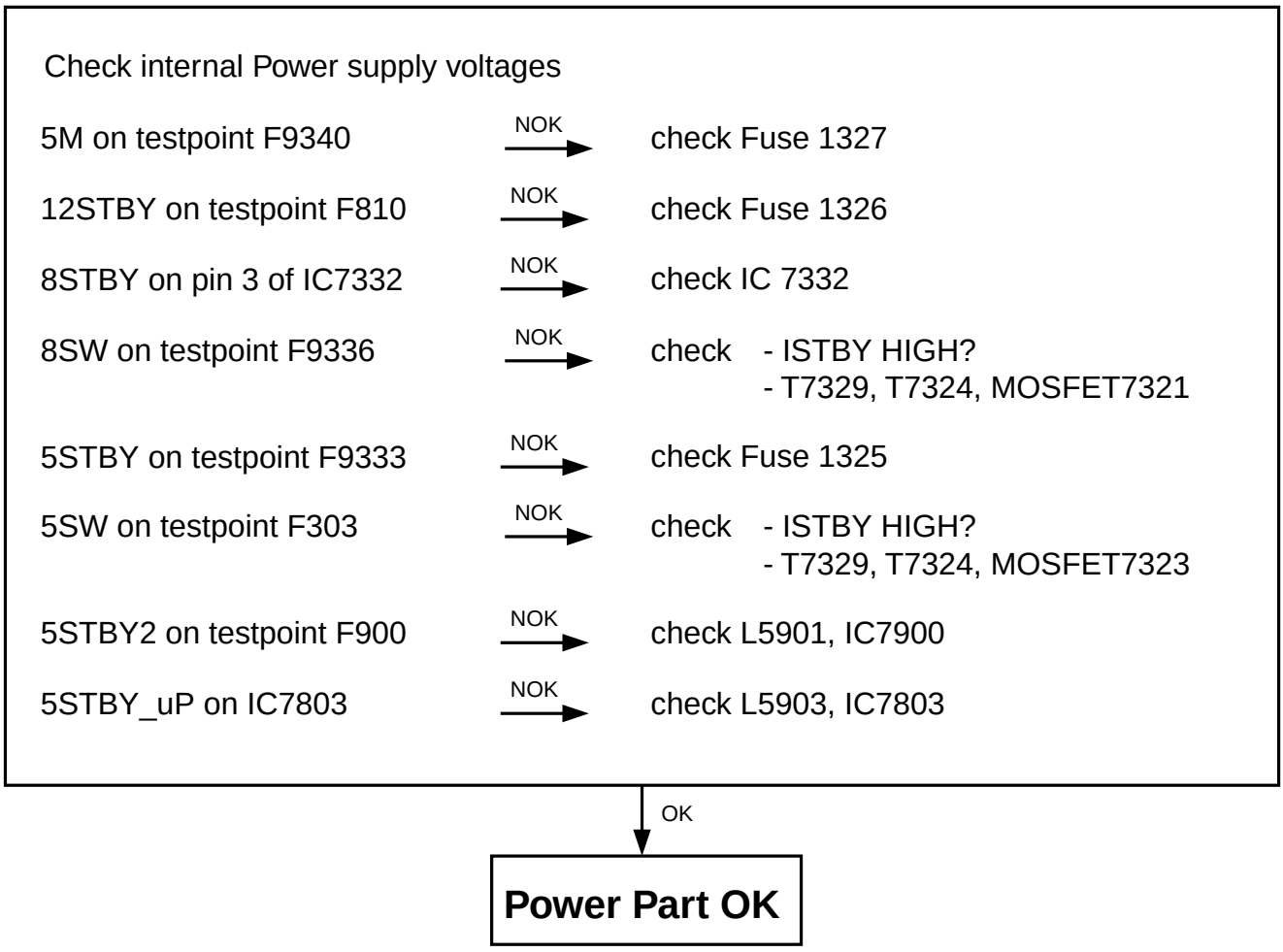


Fig. 19

4. Analog Board-5

DSW CHECK ANALOGUE BOARD

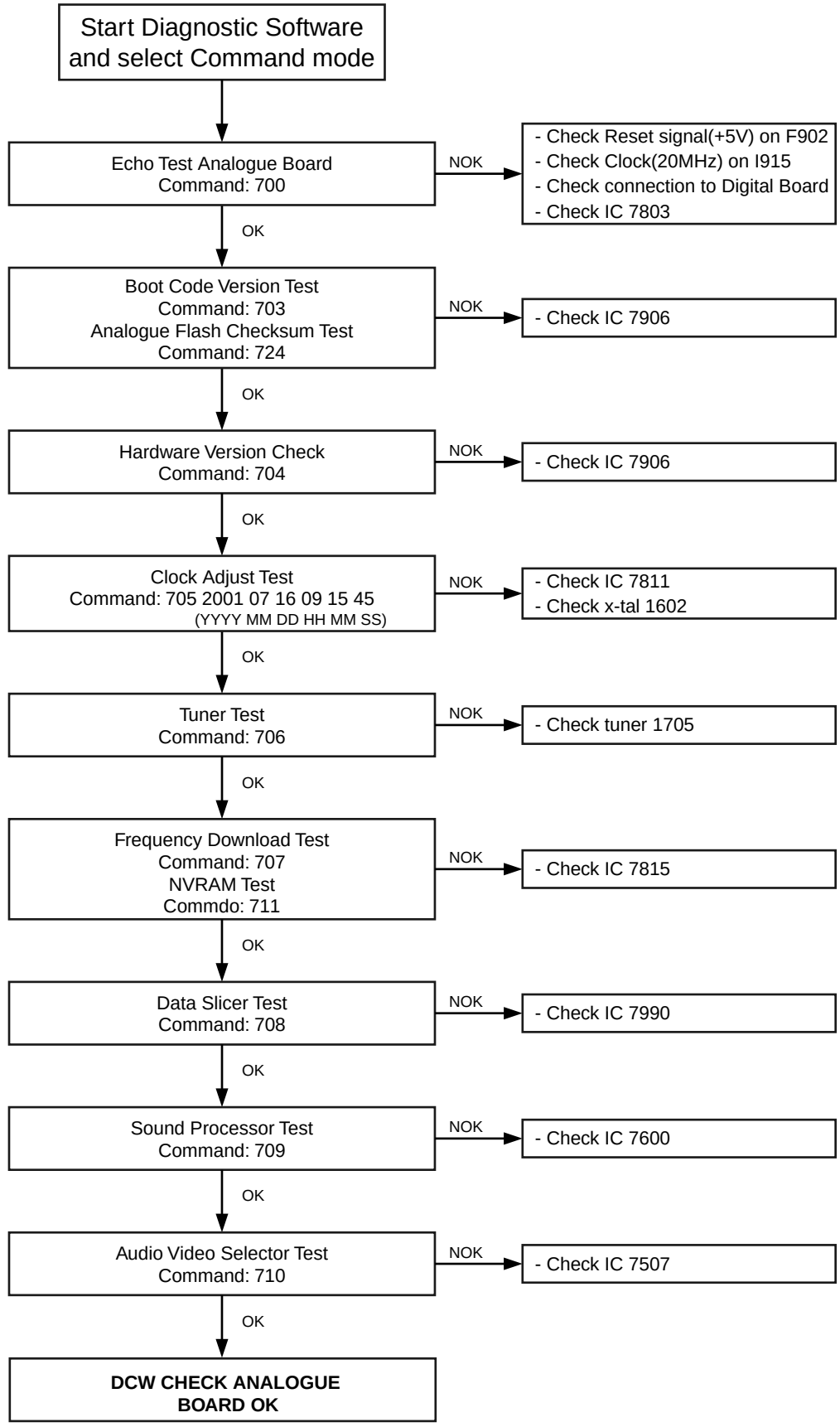


Fig. 20

4. Analog Board-6

Routing Audio and Video

Route Video

Nucleus Number: 712

Description

This nucleus routes the video signals on the analogue board to the destination determined by the input parameters.

The paths that are available for video routing and their description(Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) and will be routed to the digital board.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to SCART1 and SCART2.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to SCART1.
14	Input signals VIDEO(CVBS and Y/C) from SCART 1 will be routed to SCART2.
15	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to SCART2.
16	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to SCART2.
17	No routing
18	No routing
19	Input signals VIDEO(RGB and FAST BLANKING) from SCART2 will be routed to the corresponding pins of SCART1.
20	Signal path is routed from digital board RGB to RGB SCART1 and from RGB SCART2 to digital board YUV and from digital board CVBS to digital board CVBS.
21	Signal path is routed from digital board YC to REAR S-VIDEO(YC) OUT and from REAR S-VID-EO(YC) IN to digital board YC.

The paths that are available for video routing and their description (Nafta region) routed to the digital board.

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
05	Input signal is from YUV IN and will be routed to the digital board.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and .
09	Input signal is from YUV IN and will be routed to YUV OUT.
10	No routing.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
14	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
15	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
16	No routing.
17	Signal path is routed from digital board RGB to REAR VIDEO(YUV) OUT and from REAR VID-EO(YUV) IN to digital board YUV and from digital board CVBS to digital board CVBS.
18	Signal path is routed from digital board CVBS to REAR VIDEO(CVBS) OUT and from REAR VID-EO(CVBS) IN to digital board CVBS.
19	Signal path is routed from digital board YC to REAR S-VIDEO(YC) OUT and from REAR S-VID-EO(YC) IN to digital board YC.

Example

DD:> 712 01

71200: Video routing on the Analogue Board OK.

Test OK @

4. Analog Board-7

Route Audio
Nucleus Number: 713
Description
This nucleus routes the audio on the analogue board to the destination determined by the input parameters.
The paths that are available for audio routing and their description (Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN and will be routed to the digital board.
03	Input signal is AUDIO from SCART1 and will be routed to the digital board.
04	Input signal is AUDIO from SCART2 and will be routed to the digital board.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from AN-TENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) and AUDIO from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) and AUDIO from SCART2 and will be routed to SCART1.
11	Input signal is AUDIO from dvio board and will be routed to SCART1.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	No routing.
17	Input signal is from REAR AUDIO IN and will be routed to SCART1.
18	Input signal is from FRONT AUDIO IN and will be routed to SCART1.

The paths that are available for audio routing and their description (Nafta region)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
03	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
04	No routing.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from AN-TENNA IN and will be routed to VIDEO(CVBS) OUT and REAR CINCH OUT 2.
09	No routing.
10	Input signal is from REAR AUDIO CINCH IN 2 and will be routed to REAR AUDIO CINCH OUT 2.
11	Input signal is from FRONT AUDIO CINCH IN and will be routed to REAR AUDIO CINCH OUT 2.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	Input signal is AUDIO from dvio board and will be routed to AUDIO CINCH OUT 2.
17	No routing.
18	No routing.
19	No routing.
20	Input signal is from digital board and will be routed to the REAR AUDIO OUT 1 and input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
21	Input signal is from digital board and will be routed to the REAR AUDIO OUT 1 and input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
22	Input signal is from digital board and will be routed to the REAR AUDIO OUT 2 and input signal is from REAR AUDIO IN 1 and will be routed to the digital board.

EXAMPLE
DD:> 713 00
71300: Audio routing on the Analogue Board OK.
Test OK @

5. Display Board

TROUBLESHOOTING DISPLAY BOARD

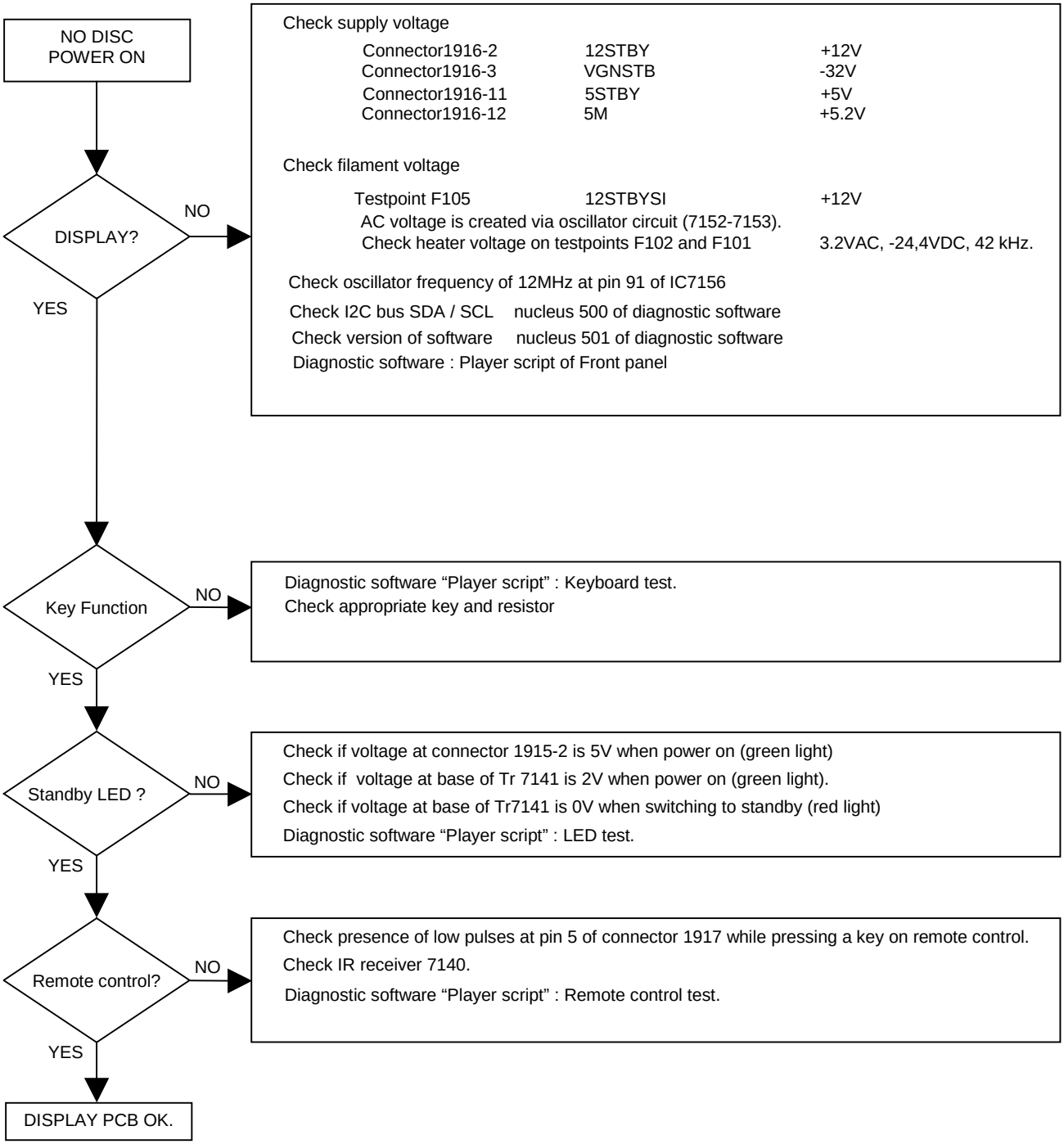

NO DISC
POWER ON
DISPLAY?
NO
YES
Check supply voltage
Connector1916-2 12STBY +12V
Connector1916-3 VGNSTB -32V
Connector1916-11 5STBY +5V
Connector1916-12 5M +5.2V
Check filament voltage
Testpoint F105 12STBYSI +12V
AC voltage is created via oscillator circuit (7152-7153).
Check heater voltage on testpoints F102 and F101 3.2VAC, -24,4VDC, 42 kHz.
Check oscillator frequency of 12MHz at pin 91 of IC7156
Check I2C bus SDA / SCL nucleus 500 of diagnostic software
Check version of software nucleus 501 of diagnostic software
Diagnostic software : Player script of Front panel
Key Function
NO
YES
Diagnostic software “Player script” : Keyboard test.
Check appropriate key and resistor
Standby LED ?
NO
YES
Check if voltage at connector 1915-2 is 5V when power on (green light)
Check if voltage at base of Tr 7141 is 2V when power on (green light).
Check if voltage at base of Tr7141 is 0V when switching to standby (red light)
Diagnostic software “Player script” : LED test.
Remote control?
NO
YES
Check presence of low pulses at pin 5 of connector 1917 while pressing a key on remote control.
Check IR receiver 7140.
Diagnostic software “Player script” : Remote control test.
DISPLAY PCB OK.

Fig. 21

6. DVIO Board-1

POWER PART CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 1 2, 3, 4 AND 5 AND DVIOTOPVIEWTESTPOINTS

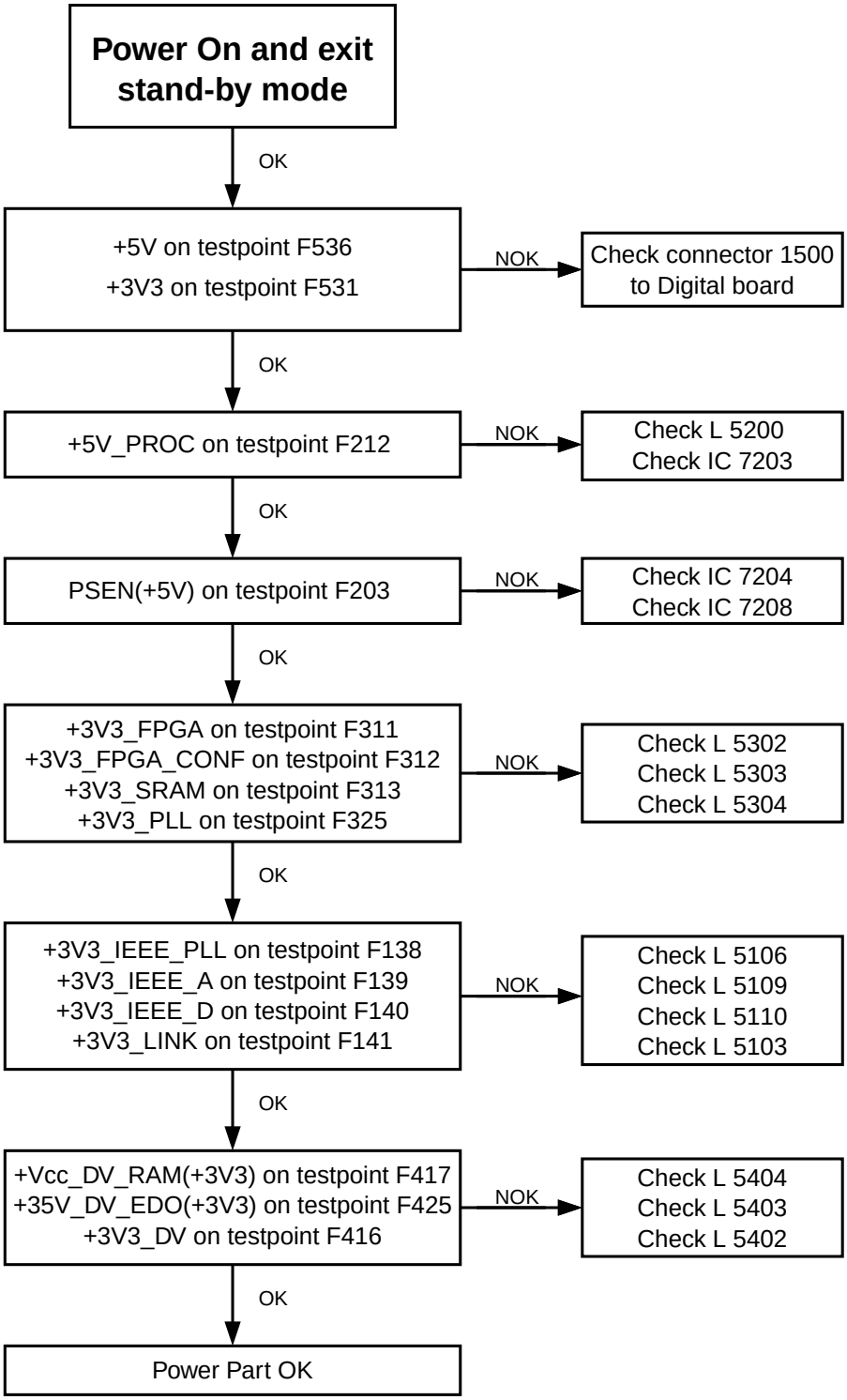


Fig. 22

6. DVIO Board-2

RESET & CLOCK CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 2, 3, 4 AND 5 AND DVIO TOP VIEW TEST POINTS

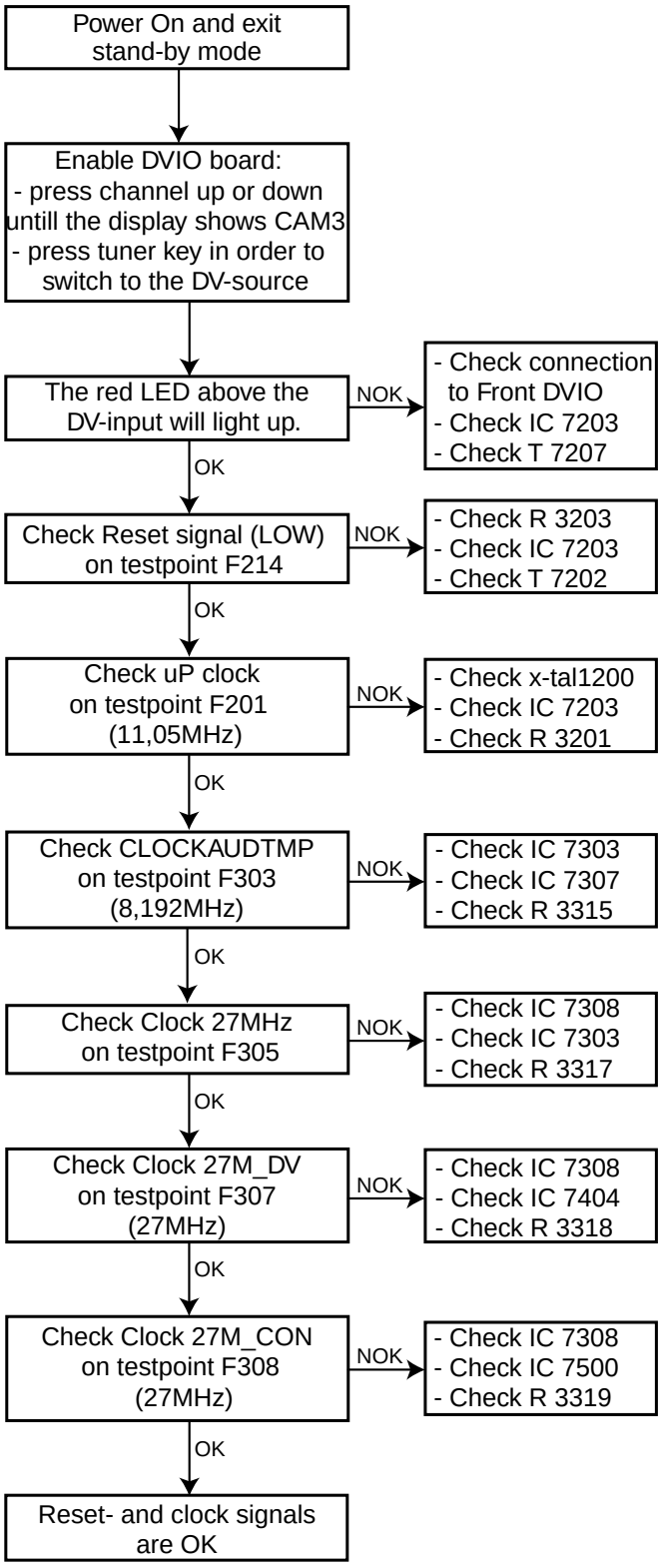


Fig. 23

6. DVIO Board-3

DSW DVIO TESTS

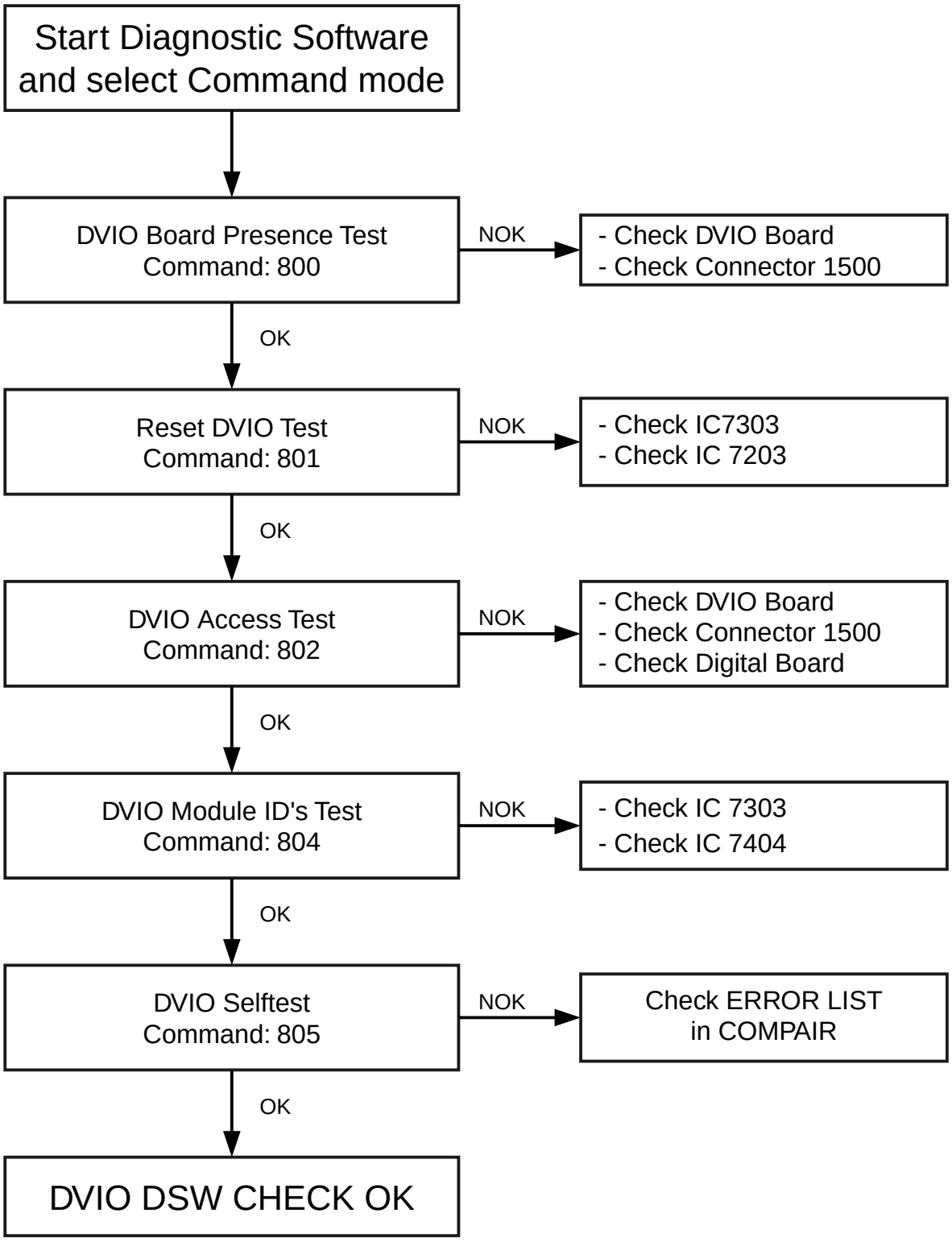
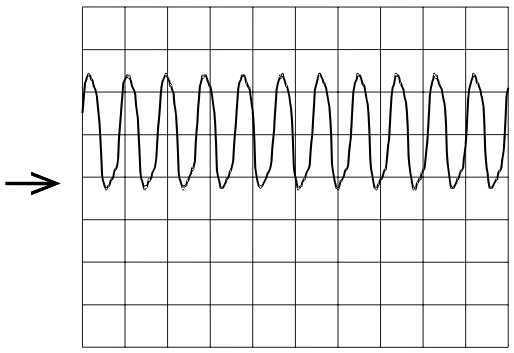


Fig. 24

6. DVIO Board-4

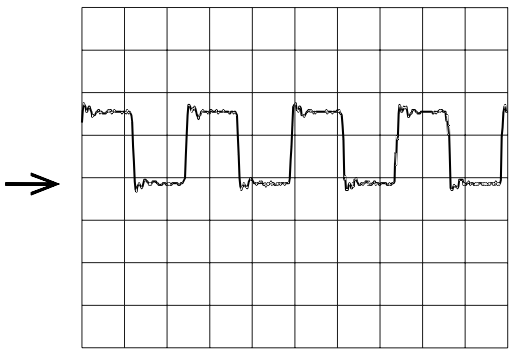
Waveforms DVIO

uP_clock



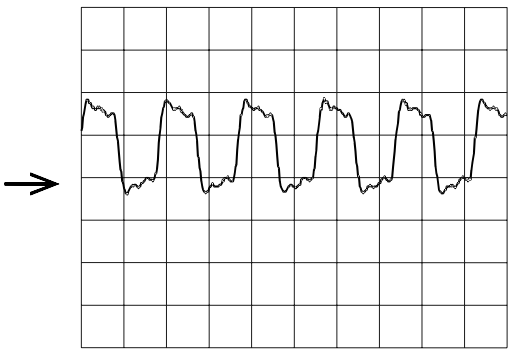
2V / div DC 100ns / div

Clockaudtmp



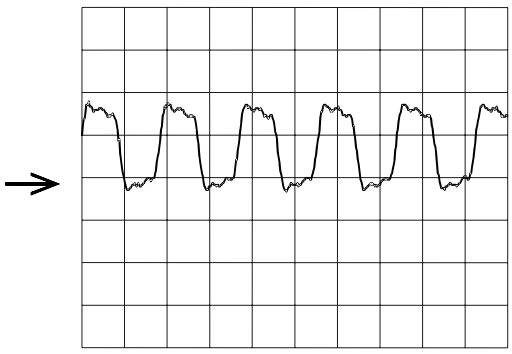
2V / div DC 50ns / div

Clock 27MHz



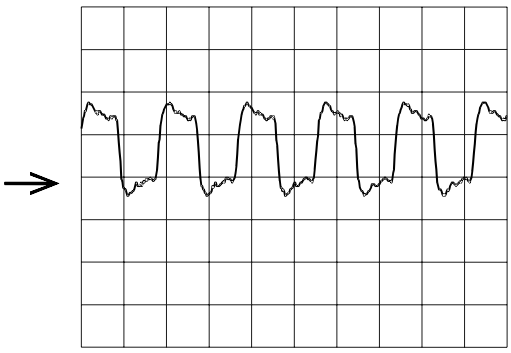
2V / div DC 20ns / div

Clock 27M_DV



2V / div DC 20ns / div

Clock 27M_CON



2V / div DC 20ns / div

Fig. 25

■ ALIGNMENTS

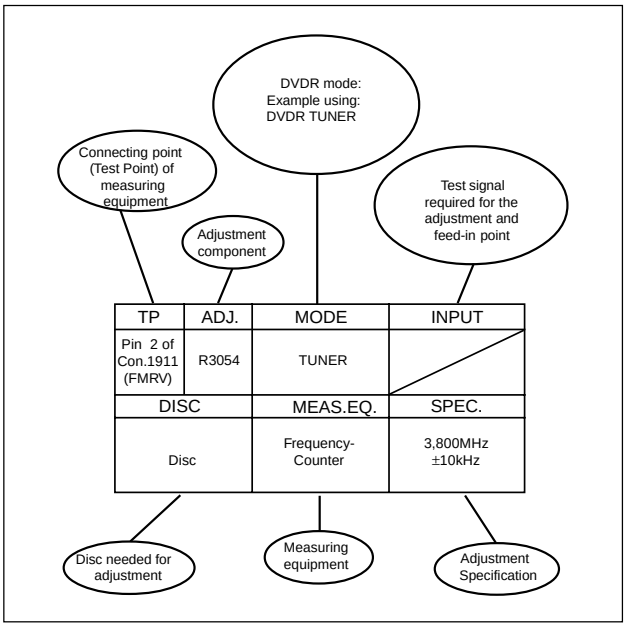
1. Alignment Instructions Analogue Board

Alignments Analog PCB Eur

ADJUSTMENT INSTRUCTIONS ANALOGUE BOARD
Test equipment:

1. Dual-trace oscilloscope
   Voltage range : 0.001 ~ 50 V/div
   Frequency : DC ~ 50 MHz
   Probe : 10:1, 1:1
2. DVM (Digital voltmeter)
3. Frequency counter
4. Sinus generator
   Sinus : 0 ~ 50 MHz
5. Test pattern generator

How to read the adjustment procedures:



Front End (FV)
Service tasks after replacement of IC 7703, coil L5702 and L5703:

1.1 AFC Adjustment:
Purpose: Correct adjustment of demodulator AFC - circuit

Symptom, if incorrectly set:
Bad or disturbed TV channel reception.

PAL - AFC adjustment [5703]:

TP	ADJ.	MODE	INPUT
IC 7703 Pin 17 (I976)	L5703	TUNER	38,9MHz 500mV$_{pp}$ at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,2V

1.2 HF - AGC adjustment [3707]:
Service tasks after replacement of IC 7703:
Purpose: Set amplifier control.

Symptom, if incorrectly set:
Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F700, IF-out)	R3707	Set tuned to channel 27	4,5mV(74dBµV) on aerial input PAL white picture, audio IF on, no modulation
DISC		MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	550mV$_{pp}$ +/-50mV (use a 10:1 probe)

1.3 Attenuating the 40.4 MHz [5702]: (SECAM only)
Service tasks after replacement of coil 5702:
Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:
Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1700 Pin 1 (F704)	L5702	TUNER	40.4 MHz, 300mV$_{rms}$ at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjust minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1700] must be smaller than the input signal amplitude by at least 5 dB.

2. Reprogramming Procedure of NVM on the Analogue PCB

The NVM, item 7815, on the Analogue board contains the following factory settings:

1. Bargraph 0dB correction factor
2. Clock correction factor
3. AFC reference value
4. Slash version

The settings 1,2 and 3 are stored in the NVM during the production of the analogue board.
The slash version is stored at the end of the production line of the set.
In case of failure, the NVM must be replaced by an empty device. By way of commands via the Diagnostic Software or via ComPair, the factory settings must be restored in the NVM.

2.1 Bargraph 0db Alignment

For an exact functionality of the bar graph in the display, a correction factor for the left and the right channel is stored in the NVM.

Procedure:

- Put the set in DSW command mode
- route Audio path from Audio front connectors to digital with the following command:
  DD:> 713 01
- apply a sine wave of 1 kHz, 1.65 Vrms (0 dB) to the front connectors, audio left and right
- store 0 dB bar graph level with command 720
  DD:>720

2.2 Clock Correction Adjustment

To guarantee an exact function of the real time clock, an adjustment of the clock frequency is possibe and stored in the NVM.

Procedure:

- Connect a pull up resistor of 10k between pin 7 and 8 of the clock IC PCF8593T, item 7811, on the analogue PCB
- put the set in service command mode
- execute command 722 to initiate that a 1 Hz signal is available on pin 7 of the clock IC
  DD:>722
- measure the frequency of the Clock Crystal with an accuracy of ±1(s. Normally the measured frequency must be between 999902 (s and 1000097 (s. If the frequency is outside this range, the clock IC must be replaced.
- Execute command 721 with the measured frequency as an input parameter
  example:
  DD:>721 1000023

2.3 AFC Reference Voltage Tuner

This function stores the reference voltage for the tuner in the NVM. Before this value can be stored, the AFC adjustment, described in the adjustment instructions of the analogue board, must be carried out.

Procedure:

- Adjust AFC circuit
- Calculate the reference value
- Execute command 732 and use the calculated reference value as parameter
  example:
  DD:>732 128

2.4 Slash Version

The slash version is stored with command 715 followed by the slash version as parameter.

Reset of Slash Version

Use command 729 to reset the analogue board to the default setting.

Procedure:

- Put the set in DSW command mode
- Execute command 729 with the following parameters:
  DD:> 729 w 0xA0 3 0x07 0xD0 0x00
- Leave the DSW command mode and start up the set in application mode No background is visible on the TV screen. The analogue board is ready to accept the appropriate slash version.

3. Rework Procedure IEEE Unique Number

3.1 Scope:

The procedure describes how to upgrade sets with a unique number after repair. This unique number is stored in the NVRAM (item 7201) of the digital board at the end of the production line.

This procedure is only valid or necessary when:

- The digital board is replaced
- NVRAM on the digital board is replaced
- NVRAM is cleared

In all other cases the repaired set retains its unique number.

The procedure defines several means to re-assure the unique number depending on the possibilities of repair or the state the faulty set is in.

3.2 Handling:

State of Original (Defective) Board:

1. The digital board starts up in Diagnostics Mode: follow procedure A to retrieve the valid unique number
2. The digital board does NOT start up in Diagnostics Mode: follow procedure B.

3.3 Procedure A

1. Connect defective digital board to PC via serial cable (3122 785 90017)
2. start up hyper terminal or any other serial terminal via the correct settings (DSW command mode interface)
3. read out existing unique number via nucleus 403
   example:
   DD:> 403
   40300: DV Unique ID = 00D7A1FC6C
   Test OK @
4. note read out
5. program new digital board via nucleus 410
   example: DD:> 410 00D7A1FC6C
   41000:
   Test OK @

The set has now the original unique number

3.4 Procedure B

1. Note the serial number of the set example:
   AH050136130156
   – AH = production centre Hasselt. According to UAW-500: A=1 and H=8
   – 05 = change code (this is not used for this calculation)
   – 01 = YEAR
   – 36 = Production WEEK
   – 130156 = Lot and SERIAL number
2. Calculate the unique number: this number always exists out of 10 hexadecimal numbers.
3. First 5 numbers: First we calculate a decimal number according to the formula below: 35828*YEAR + 676* WEEK + 26*A + H + 8788 The figures are fixed, YEAR + WEEK + factory code (A + H) are variable
   Example: 35828*01+676*36+26*1+8+8788 = 68986 (decimal) Then we translate the decimal number to a hexadecimal number.
   example: 68986 (decimal)= 10D7A (hex)
4. Last 5 numbers: The last 5 numbers exist out of the Lot and SERIAL number. We have to translate the decimal number to the next 5 hexadecimal numbers:
   Example: 130156 (decimal) = 1FC6C (hex)
5. Program new digital board via nucleus 410 Therefore we use the 10 hexadecimal numbers we calculated above:
   example:
   DD:> 410 10D7A1FC6C
   41000:
   Test OK @

The set has now its original unique numbe

■ CIRCUIT DESCRIPTION

1. Multi-Mode SOPS 50PS203

1.1. Why Multi-Mode SOPS?

Using ordinary SOPS results in a decrease of the efficiency at low output loads due to the increase of the switching frequency.
The Multi-Mode SOPS will reduce the switching frequency at low loads but still preserves valley switching.

1.2. Block Diagram

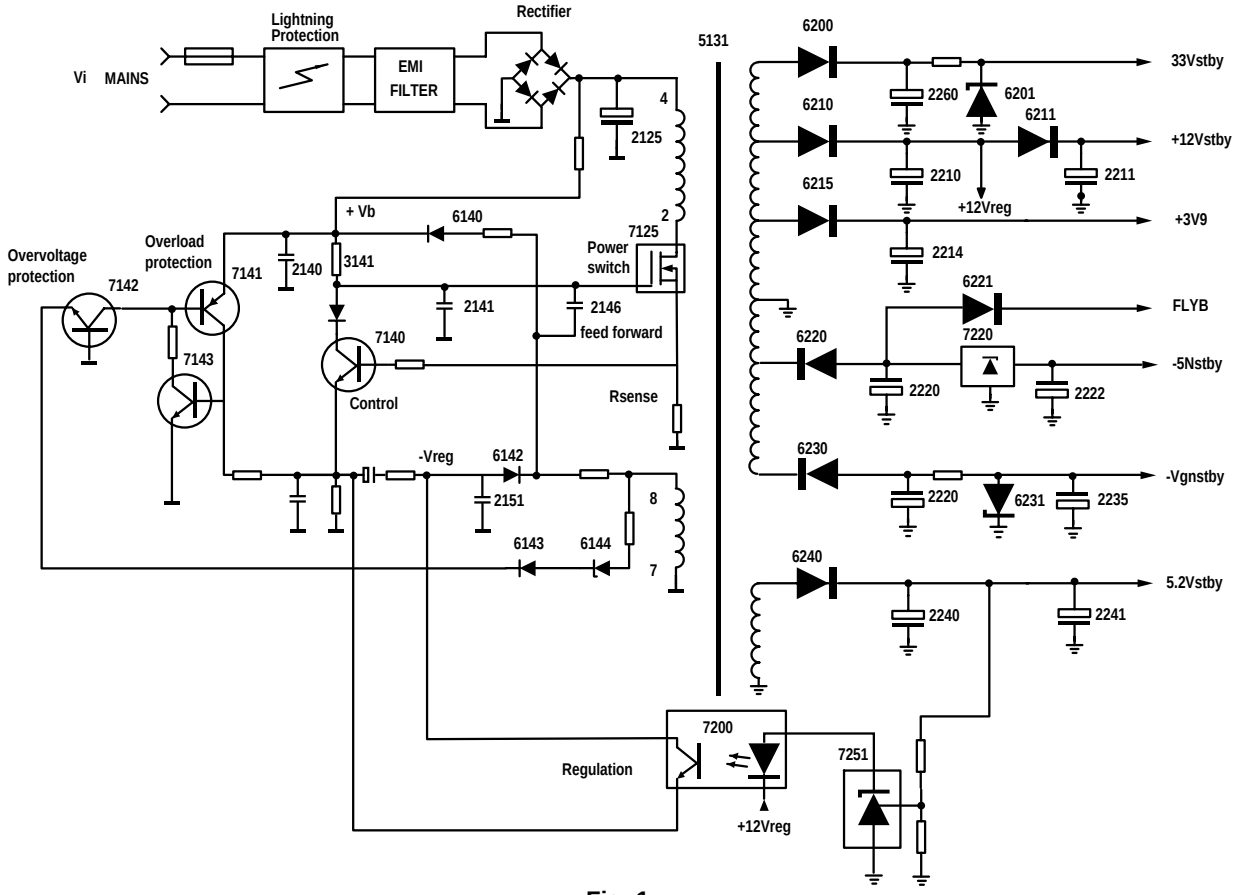


Fig. 1

1.3. Circuit Description

Input Circuit

The input circuit consists of a lightning protection circuit and an EMI filter.
The lightning protection comprises R3120, sparkgaps 1124 and 1125. D6128, 6129, C2127 and R3129 are optional.
L5110, L5115, C2120 and L5120 form the EMI filter. It prevents inflow of noises into the mains.

Primary Rectifier/smoothing Circuit

The AC input is rectified by diodes 6151,6152, 6153, 6154 and smoothed into C2125. The voltage over C2125 is approximately 300V. It can vary from 200V to 390V.

Start Circuit

This circuit is formed by R3125, 3126, R3141, C2140 and R3132.

When the power plug is connected to the mains voltage, the MOSFET 7125 will start conducting as soon as the gate voltage reaches a treshold value. A current starts to flow in primary winding 2-4. The MOSFET will be fed forward via winding 7-8, R3150 and C2146.

+Vb Supply and Negative Regulation Voltage

The positive part of the voltage over winding 7-8 will be rectified via R3150, D6140 and charged via R3140 into C2140. The voltage over C2140 has a value of +30 till +40V. This value depends on the value of the mains voltage Vi and the load.
The negative part of the voltage over winding 7-8 will be rectified via R3150, D6142 and charged into C2151. The voltage over C2151 has a value of -15V and is used as regulation voltage.

Control Circuit

The control circuit exists of T7140, D6141, C2144 and 2145, C2147, R3147 and 3148.

This circuit is fed by supply voltage +Vb via R 3141. This circuit controls the conduction time and the switching frequency of the power switch circuit. It switches off the MOSFET as soon as the voltage over Rsense reaches a certain value. This value depends on the error voltage at the emittor of T7140, which can be positive or negative (+/ - 0,66V). The voltage fed back by the regulation circuit defines this error voltage.

Power Switch Circuit

This circuit comprises MOSFET 7125, Rsense formed by R3133, 3134, 3135, 3136 and 3137, R3131, R3132, D6146.

Diodes 6130, 6131 and 6132 protect the control circuit in case of failure of the MOSFET.

Regulation Circuit

The regulation circuit comprises opto-coupler 7200, which isolates the base voltage of transistor 7140 at the primary side from a reference component 7251 at the secondary side. The TL431(7251) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

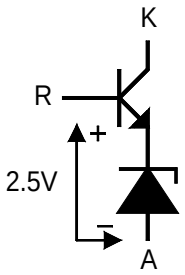


Fig. 2

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero.

The cathode current flows through the LED of the opto-coupler.

The collector current of the opto-coupler will adjust the feedback level of the error voltage at the emittor of T7140.

Overload Protection Circuit

This circuit consists of R3145, C2143, a thyristor circuit formed by T7141 and T7143, R3143 and R3142. When the output is shortened, the thyristor circuit will start to conduct and switch off the supply voltage over C2140. This results in a switching off of the drain current of the MOSFET 7125 and the output will be disabled. The start circuit will try to start up the power supply again. If the circuit is still shortened, the complete start and stop sequence will repeat. The power supply comes in a hiccup mode (is ticking).

Overvoltage Protection Circuit

This circuit consists of R3149, D6144, 6143, R3144, C2142 and T7142.

When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 7-8.

When an overvoltage is detected, the circuit will start up the thyristor circuit T7141-7143. The power supply will come in a hiccup mode as long as the error in the control loop is present.

Secondary Rectifier/Smoothing Circuit

There are 6 rectifier/smoothing circuits on the secondary side.

Each voltage depends on the number of windings of the transformer.

From these circuits a lot of voltages are derived and fed to 3 connectors. The following voltages are present at the output: Connector 209

Functional use: to Digital board + Dvio board

1. +3V3(for dig pcb + DVio)
2. +3V3(for dig pcb + DVio)
3. +3V3(for dig pcb + DVio)
4. +3V3(for dig pcb + DVio)
5. GND(for dig pcb + DVio)
6. +12V(for dig pcb + DVio)
7. GND(for dig pcb + DVio)
8. GND(for dig pcb + DVio)
9. +5V(for dig pcb + DVio)
10. STBY control(for dig pcb + DVio)
11. GND(for dig pcb + DVio)
12. -5V(for dig pcb + DVio)

The +12V is switched off by the STBY_ctrl signal.

When the +12V is switched off, also the +3V3, +5V and -5V are switched off. All these voltages are low drop regulated.

Connector 0205

Functional use: to analogue board + display board + flap motor 'STBY' indicates that the voltage will not be switched off in the standby situation.

1. +12VSTBY(= +12V Standby, for display heating, 8Vstby)
2. +5VSTBY(= +5V Standby; general use)
3. -5NSTBY(= -5V Standby; neg. voltage for drivers)
4. VGNSTBY(= -32V Standby; for display grids)
5. +33STBY(= +33V Standby; for tuner)
6. FLYB(flyback pulse for power fail + measurement)
7. GNDA(Ground for the analogue board)

Connector 0207

Functional use: to engine

1. +3V3(for engine servo board)
2. +5V(for engine servo board)
3. GND(for engine servo board)
4. +4V6E(for engine analog part)
5. GND(for engine servo board)
6. -5V(for engine servo board)
7. GND(for engine motor currents)
8. +12V(for engine motor currents)

2. Display Board

2.1 Operation Unit DC (DC Part)

The core element of the operation unit DC is the microcontroller TMP88CU77ZF [7156]. The TMP88CU77ZF is an 8 bit microcontroller fitted with 96kB ROM and 3kB RAM and is responsible for following functions:

- Integrated VFD driver
- Timer
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver pos. 6170
- Activation of the display
- Motor driver

The system clock is generated with the 12MHz quartz (Pos. 1153).

2.2 Evaluation of the Keyboard Matrix

There are 15 different keys on the display board. A resistor network is used to generate a specific direct voltage value, depending on the key pressed, via the resistors 3145, 3171, 3183 and 3194 on the analog/digital (A/D) ports (7156 Pin 17, 18, 19, 20). Pressing keys simultaneously may lead to undesired functions!

2.3 IR Receiver and Signal Evaluation

The IR receiver [7140] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received transmission (approx. 940nm) in electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7140], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is input into the controller for further signal evaluation via input IRR [7156, pin 2].

2.4 Motor Driver Flap

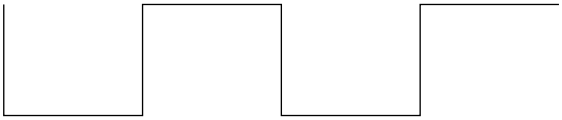
The flap-motor is controlled via the 2 Port-Pins (MD1, MD2) of the P (7156, Pin 12, Pin 100). The motor driver part is constructed as a bridged dual power operational amplifier.

Between the IC outputs (7120, Pin1, Pin3) and a Boucherot circuit (2121, 3126) suppresses a spurious 3MHz oscillation from the output stage. The two ports-pins (MD1, MD2) of the P are PWM-outputs and are controlled in the following way:

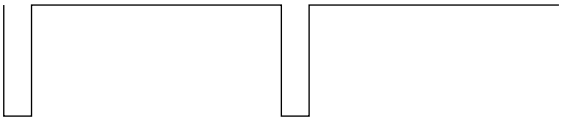
Flap Motor:

	MD1	MD2
off	H	L
open	H	PWM(H)
close	L	PWM(L)

Duty Cycle 50% for OPEN and CLOSE



Duty Cycle app. 10% for CLOSE



Duty Cycle app. 10% for OPEN

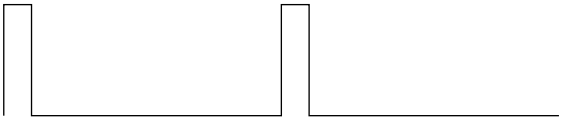


Fig. 3

For the detection of the end-positions of the flap there are two switches (1178, 1179) installed and the information is evaluated from the P via the signals SW_1178 and SW_1179.

Flap Switches:

	SW1	SW2
open	L	H
closed	H	L
moving	H	H
error	L	L

2.5 Bi-Color LED (Standby and ON)

The STBY-LED is a red/green bi-color-LED and is controlled via the STBYLED-signal of the P (7156 Pin 10) in the following way:

Colour of STBY LED	Status of the Set
red	STBY
green	ON

3. Analog Board Europe (A, B, G models)

3.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the
following functions:

- A/D converters
- composite sync input
- I^2C bus interface

Following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900).
The system clock is generated with the 20MHz quartz (Pos. 1994).

3.2 Bus Systems

The communication between the P and the other functional groups is via the I^2C-bus (SDA, SCL). The clock rate is approx. 95kHz.
Functional groups on the I^2C bus:

- E^2PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)
- VPS-IC (Pos. 7990).

3.3 E^2PROM

The E^2PROM ST24E16 (Pos. 7815) is an electric erasable and programmable, non-volatile memory. The E^2PROM stores data specific to the device, such as the AFC-reference value, clock-correction- factor, etc. The data is accessed by the P via the I^2C-bus.

3.4 VPS, PDC, Teletext (Europe Only)

The STV5348 (Pos. 7990) is a VPS, PDC, and Teletext Decoder with an external 13,875Mhz quartz.
The following data formats are identified:

- VPS (Timer data and station name)
- PDC Format 2 (Timer data and station name)
- PDC Format 1 (station name and time)
- TXT header line (time for „time download“)

3.5 FOME

The FOME-circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

3.6 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25° C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40° C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

3.7 Power Supply

The 5SW and 8SW supply are switched off in case of standby from the P via the ISTBY-line. This is possible for power-save.
The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

3.8 Front End (TU, AP Part)

The Front End Comprises the Following Parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9818 [7703]
- Sound processor MSP3415G [7600]

IF Selection

The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (33.9 MHz).
A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1700], [1701] for video, [1702] for audio. [1700] Is switched into the signal path for DK/I-SECAM L/L' reception, if the signal SAWS is “high”. In this case the switches [7701], [7702] are open and the diode [6700] is conducting. [1701] is switched into the signal path for BG reception, if the signal SAWS is “low”. Then the switch [7708] is open and the diode [6701] is conducting. For DK/I-SECAM L/L' reception, an additional circuit for suppressing the adjacent channel audio carrier is provided, which is set using coil [5702] to maximum suppression at 40.4MHz.

IF Demodulator

TDA 9818

The IF signal from the tuner is processed by the demodulator IC TDA 9818 [7703]. The signal PSS to pin3 switches between demodulation of positive SECAM and negative PAL modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L’. If the signal SB1 is “high”, the switch [7707] is closed and the diode [6702] is not conducting. For all other standards the diode [6702] is conducting and the switch [7707] is open. The output signal from this SAW filter is first processed in the TDA 9818. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9818 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9818 is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3702] to earth. The switch [7700] and the signal SB1 "high" do this. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV), the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703].
The demodulator AGC voltage at pin4 is used to

determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid cross talk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video for BG standards. For all other standards the switch [7704] and signal TS "low" bypass this trap. In this cases the selectivity of the SAW filter [1700] is sufficient. A frequency response correction is achieved by the inductance [5009] for not BG standards. This correction is not preferred for SECAM L' and therefore shorts circuited by [7709], if the signal SB1 is “high”. The demodulated video signal VFV is available after the buffer and limiting stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9818 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3415G

The MSP 3415G [7600] is a multistandard sound processor which can demodulate FM Mono/Stereo, NICAM and AM signals. The incoming signal is first controlled and then digitised. The digital signal is then demodulated in 2 separate channels. In the first MSP channel, FM and NICAM (B/G/I/D/K) are demodulated, whereas in the second MSP channel, FM and are demodulated again (NICAM L corresponds to NICAM B/G). These demodulated signals are selected digitally in the I/O and switched to the D/A converter on the outputs. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

3.9 Input/Output Video-Routing (A, B, G models)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A. It is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS switches, three chroma switches and one RGB switch. All switches have 6-dB amplification on the outputs.

The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB inputs have bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus. The IC has also one slow blanking monitor and one fast blanking switch for fast RGB insertion (see detailed description in chapter 1.5). Two pre-selectors BA 7652 are additionally used: One for switching between Rear CVBS, Y- Rear and Front, the second for switching between Chroma- Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are four CVBS input connection possibilities: Front chinch (E6), Rear Chinch (E4), Scart 1 (E1) and Scart 2 (E2). Rear Chinch In is routed via the pre selector BA 7652; the other signals are connected direct to the STV 6410. The selected CVBS signal is routed to Rear Chinch Out (via BA 7660, 6dB amplification, 75 Ohm driver) and to Scart 1. Independent of the input signal quality (CVBS, S-Video or RGB) the digital board supplies also S-Video and RGB signals to the corresponding socket.

S-Video Signals:

There are also four S-Video input connection possibilities: Front In (E5), Rear In (E3), Scart 1 and Scart 2. For S-Video from Scart this option has to be switched on in the OSD menu.

The pre-selectors and the STV 6410 do the signal selection (for detailed routing see overview). Also the video quality will be S-Video, the digital board supplies also CVBS to the corresponding sockets. The S-Video signal that is coming from the digital board is routed via BA 7660 (6-dB amplification and 75-Ohm driver) to the S-Video Rear Out socket.

RGB Signals:

The Scart 2 RGB input signal (Decoder socket) is connected to the RGB switch of STV 6410 and to the digital board in parallel.

The RGB from Scart 2 is routed to Scart 1 in low power standby mode. The direct connection (not via STV 6410) is for loop through and REC. The RGB signal, which is coming from the digital board, is connected to the RGB encoder input of the STV6410 and is routed to Scart 1 in all other modes.

As the Scart-connection can carry either RGB- or Y/C-signals it is necessary to define the available and selected signal-property.

While Pin15 of Scart (Red or Chroma-upstream) is fully handled via STV6410A the Pin7 (Blue or Chroma-downstream) has to be extra set.

- Scart1: Pin42 of C (SC1YC_H-line):
  – Low (Blue-Out on SC1
  – High (Chroma-In on SC1
- Scart2: Pin41 of C (SC2RGB_H-line):
  – Low (Chroma-Out on SC2
  – High (Blue-In on SC2

Detection of Status-Information

Pin-8 (Slow-Blank):

Level-detection of Pin-8 (Scart-1 and -2) is realised by using STV6410A. It can be readout via IIC-Bus by the CC-C. To obtain the status of Scart1-Pin8, Bit 0 & 1 of register 06h must be set to 0 (Input-mode). The corresponding bits for verification of Scart2-Pin8-status are set to input-mode as default.

Meaning of Read-Register-Bits:

- Bit 7 & 6: not used
- Bit 5 & 4: Status Scart-2/Pin8:
  – 0 1 Low-level
  – 1 0 Medium-level (16:9)
  – 1 1 High-level (4:3)

- Bit 3 &2: not used
- Bit 1 & 0: Status Scart-1/Pin8:
  – 0 1 Low-level
  – 1 0 Medium-level (16:9)
  – 1 1 High-level (4:3)

Pin-16 (Fast Blank):
Only the status/level of Scart-2/Pin16 must be detected; this is realised by using PortC3/AIN14 (Pin25) of the CC-C as an Analogue-input.
- ADC-value lower or equal 24h (Pin16 low (no RGB-signals)
- ADC-value greater 24h (Pin16 high (RGB present on Scart-2)

To avoid misdetection a “software-integration” (result is first valid if it was 3-times the same) must be implemented, determination has to be done approx. every 47msec (no multiple of V-sync).

WSS on Y/C-Plug:
Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.
- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on plug

Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information
Pin-8 (Slow Blank):
Only on Scart-1 the Slow-Blank-Status (Level of Pin8) must be created, which is done via IIC-Bus-register 06h (Bits 0 & 1) of the STV6410A.

Pin-16 (Fast Blank):
Only the status/level of Pin16-Scart1 must be controlled; this is realised by using the FB-switch-capabilities of the STV6410A, which are set via IIC-Bus-register 04h (bits 4 & 5).

WSS on Y/C-Plug:
The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).
- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

3.10 Audio Routing Analogue board (Europe / Nafta)
General Description:
The Audio- I/O switching is realised by the STV6410 I/O switch.
By I²C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).
Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC´ s. For further processing, the UDA 1360TS (ADC) delivers the data-in I²S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I²S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:
The STV 6410 is an I²C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms.
The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:
The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.
The UDA supports the I²S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.
The device is able to handle system clocks of 256fs and 384fs.
Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:
The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.
The UDA 1328 supports the I²S-bus data format with word lengths of up to 24 bits.
Digital sound features can be controlled with the L3 interface.
System clock can be set to 256fs or 384fs.
The Device also provides 2 high quality differential outputs.
Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.
Supply voltage is 3V3.

Detailed Description MC 33078:
The MC33078 is a dual operational amplifier for audio applications.
It offers low voltage noise (4.5nV / $\sqrt{Hz}$) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).
In addition the MC33078 has a very low distortion (0.002%).

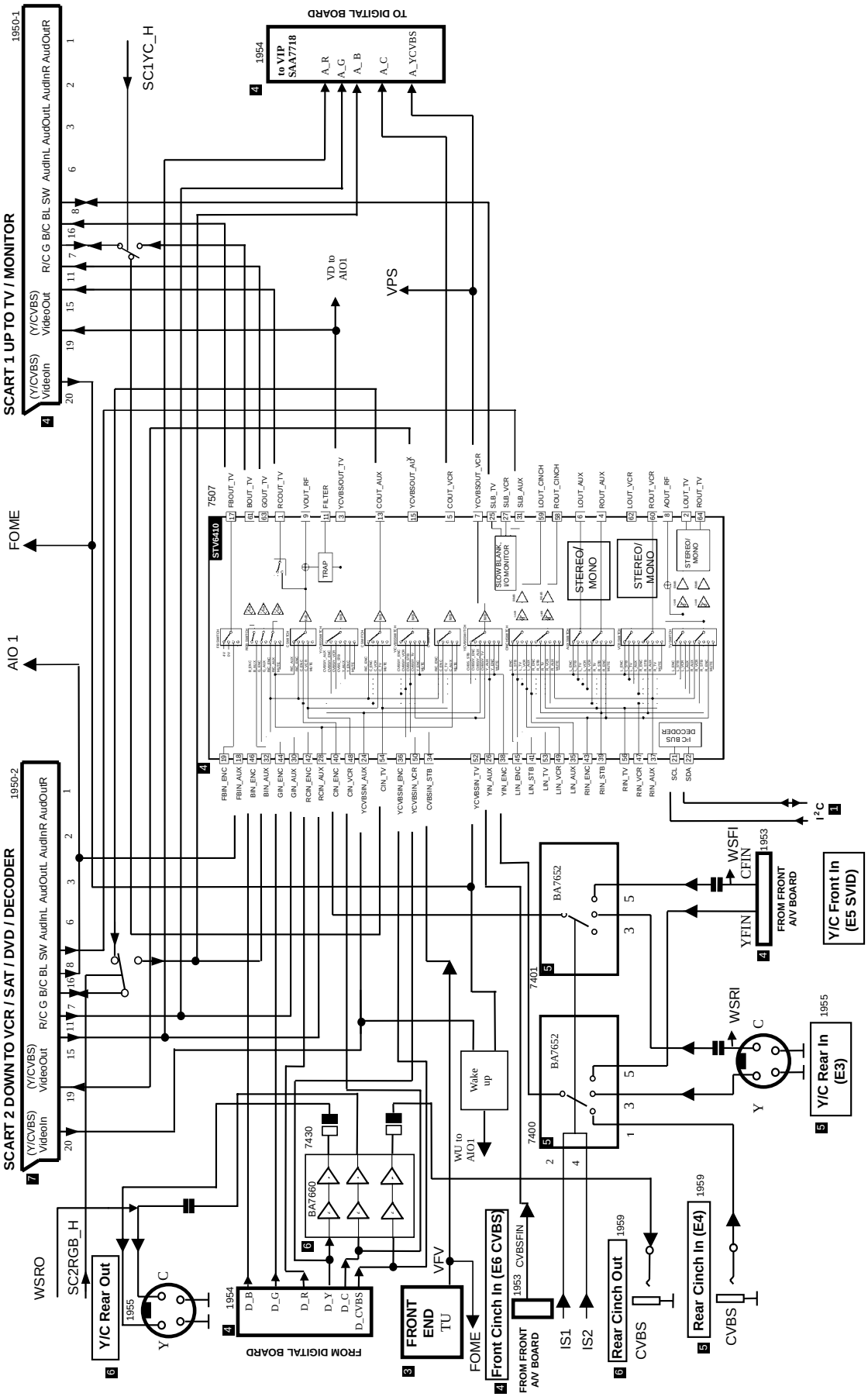

SCART 1 UP TO TV / MONITOR
SCART 2 DOWN TO VCR / SAT / DVD / DECODER
TO DIGITAL BOARD
to VIP SAA7718
A_R
A_G
A_B
A_C
A_YCVBS
SC1YC_H
VD to AIO1
VPS
FOME
AIO 1
STV6410
7507
TRAP
FILTER
SLOW BLANK I/O MONITOR
STEREO/ MONO
I²C BUS DECODER
SCL
SDA
I²C
WU to AIO1
Wake up
BA7652
7401
7400
BA7660
7430
WSFI
CFIN
YFIN
FROM FRONT A/V BOARD
Y/C Front In (E5 SVID)
WSRI
Y/C Rear In (E3)
WSRO
SC2RGB_H
Y/C Rear Out
FROM DIGITAL BOARD
D_B
D_G
D_R
D_Y
D_C
D_CVBS
FRONT END TU
VFV
FOME
Front Cinch In (E6 CVBS)
CVBSFIN
IS1
IS2
Rear Cinch Out
Rear Cinch In (E4)
CVBS

Fig. 4

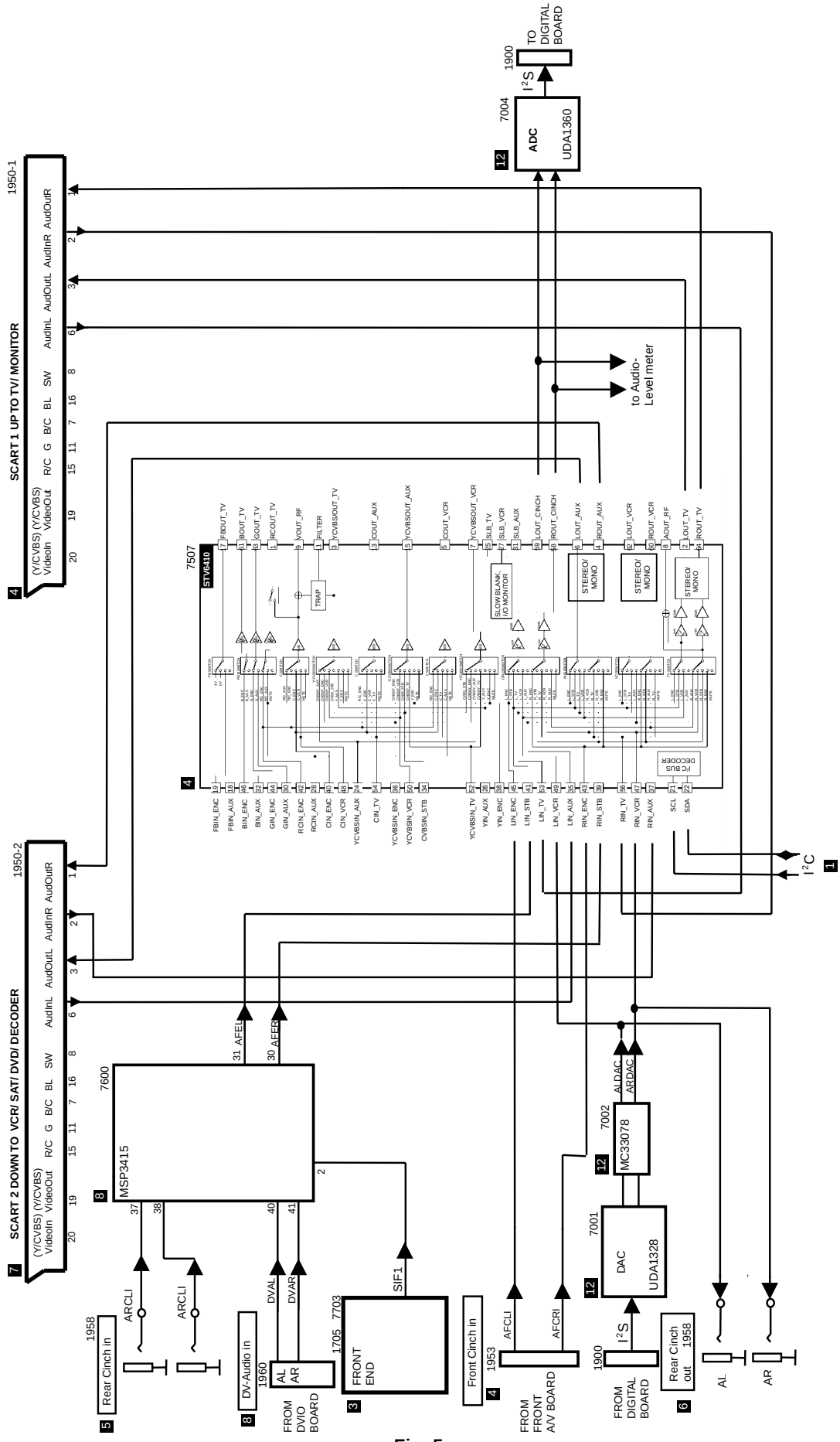

SCART 1 UP TO TV/ MONITOR
SCART 2 DOWN TO VCR/ SAT/ DVD/ DECODER
(Y/CVBS) (Y/CVBS)
VideoIn VideoOut
R/C G B/C BL SW AudInL AudOutL AudInR AudOutR
1950-1
1950-2
7507
STV6410
7600
MSP3415
7004
ADC
UDA1360
7002
MC33078
7001
DAC
UDA1328
7703
FRONT END
1900
TO DIGITAL BOARD
I2S
to Audio-Level meter
STEREO/ MONO
SLOW BLANK I/O MONITOR
TRAP
I2C BUS DECODER
I2C
AFEL
AFER
ALDAC
ARDAC
ARCLI
DVAL
DVAR
SIF1
AFCLI
AFCRI
Rear Cinch in
DV-Audio in
FROM DVIO BOARD
Front Cinch in
FROM FRONT A/V BOARD
FROM DIGITAL BOARD
Rear Cinch out
AL
AR

Fig. 5

4. Analog Board Nafta version

4.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I^2C bus interface

The following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900).

The system clock is generated with the 20MHz quartz (Pos. 1994).

4.2 Bus Systems

The communication between the P and the other functional groups is via the I^2C-bus (SDA, SCL). The clock rate is approx. 95kHz.

Functional groups on the I^2C bus:

- E^2PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)

4.3 E^2PROM

The E^2PROM ST24E16 (Pos. 7815) is an electric erasable and writeable, non-volatile memory. The E^2PROM stores data specific to the device, such as the AFC-reference value, clock-correction- factor, etc. The data is accessed by the P via the I^2C-bus.

4.4 FOME

The FOME (Follow Me) -circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

4.5 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25° C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40° C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

4.6 Power Supply

The 5SW and 8SW supply are switched off in case of Stby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

4.7 Front End (TU, AP Part)

The front end comprises the following parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9817 [7703]
- Sound processor MSP3445G [7600]

IF Selection

The IF frequency of the video carrier is 45.75 MHz. A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1701] for video, [1702] for audio.

IF Demodulator

TDA 9817

The IF signal from the tuner is processed by the demodulator IC TDA 9817 [7703]. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9817 is adjusted so that when a frequency of 45.75 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9817 is 2.5V. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV) the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703].

The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid crosstalk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video. The demodulated video signal VFV is available after the buffer and limiter stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9817 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3445G

The MSP 3445G [7600] is a NTSC sound processor. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

4.8 Video-Routing (Nafta Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A, which is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS, three chroma, and one RGB switch which is not used in the Nafta I/O. All switches have 6-dB amplification on the outputs. The YCVBS inputs

have bottom clamp, the chroma inputs have average clamp, and the RGB switch has bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus.
Two pre-selectors BA 7652 are additionally used: One for switching between Y- Rear and Front, the second for switching between Chroma- Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:
There are two CVBS input connection possibilities: Front chinch (E5) and Rear Chinch In (E3). Both CVBS sources are connected direct to the STV 6410 and routed to Rear Out 1 and Rear Out 2 via the 75-Ohm driver BA 7623. Both CVBS output sockets are connected to BA 7623 in parallel.
Independent of the input signal quality (CVBS, S-Video or Y/UV) the digital board supplies also S-Video and Y/UV signals to the corresponding sockets.

S-Video Signals:
There are also two S-Video input connection possibilities: Front (E4) and Rear (E2) S-Video In which are connected to the pre-selector IC's BA 7652. One is used for Y, the other for Chroma switching. The output of the pre-selector switches is connected to the STV 6410, and then the signal is routed via the 75-Ohm driver BA 7623 to the Rear Out S-Video socket.
Also the video quality will be S-Video, the digital board supplies also CVBS and Y/UV to the corresponding sockets.

Y/UV Signals:
The Y/UV In signal is routed direct to the digital board, there is no Y/UV IN -> Y/UV Out loop through in low power standby. As the digital board supplies only RGB signals, a RGB Y/UV matrix is used. This matrix consists of the operational amplifier TSH95 which generates the U and V signals according the formulas: 2U=B-0,338R-0,661G, 2V=R-0,838G-0,161B. Then the signals are routed to the UV Output sockets via the 75-Ohm driver BA 7623. The corresponding Y signal is coming from the digital board via the STV 6410. The 75 Ohm Y socket is driven by the 75-Ohm driver BA 7623 and finally connected to the of the Y/UV Output.

Detection of Status-Information
WSS on Y/C-Plug:
- Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.
- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on plug
- Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information
WSS on Y/C-Plug:
The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).
- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

4.9 Audio routing Analogue board (Europe / Nafta)
General Description:
The Audio- I/O switching is realised by the STV6410 I/O switch.
By I^2C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).
Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC´ s. For further processing, the UDA 1360TS (ADC) delivers the data-in I^2S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I^2S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:
The STV 6410 is an I^2C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms.
The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:
The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.
The UDA supports the I^2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.
The device is able to handle system clocks of 256fs and 384fs.
Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:

The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA 1328 supports the I^2S-bus data format with word lengths of up to 24 bits.

Digital sound features can be controlled with the L3 interface.

System clock can be set to 256fs or 384fs.

The Device also provides 2 high quality differential outputs.

Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.

Supply voltage is 3V3.

Detailed Description MC 33078:

The MC33078 is a dual operational amplifier for audio applications.

It offers low voltage noise (4.5nV / $\sqrt{Hz}$) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).

In addition the MC33078 has a very low distortion (0,002%).

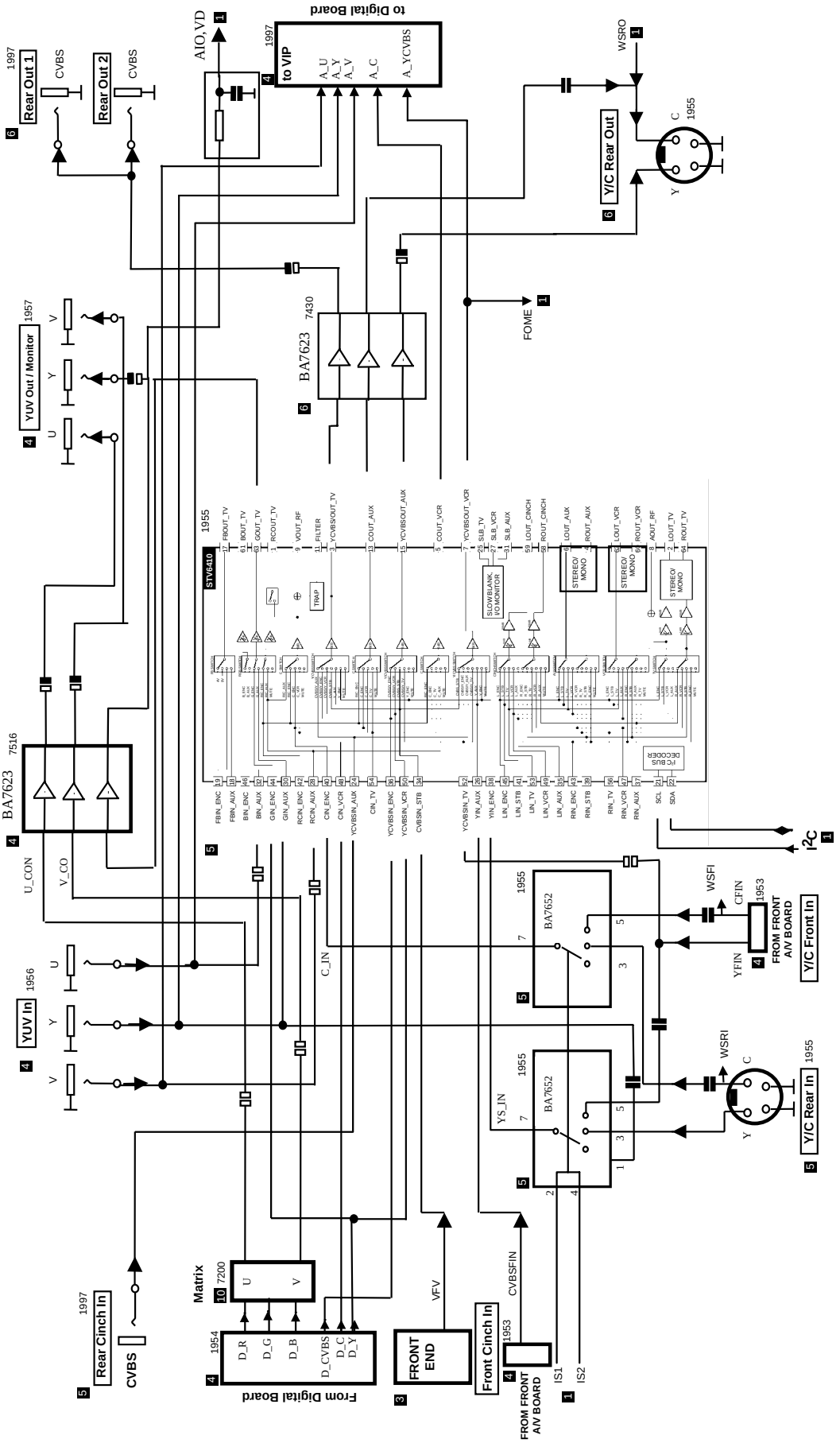

to Digital Board
AIO,VD
to VIP
A_U
A_V
A_C
A_YCVBS
Rear Out 1
Rear Out 2
CVBS
YUV Out / Monitor
Y/C Rear Out
WSRO
FOME
BA7623
STV6410
SLOWBLANK I/O MONITOR
TRAP
STEREO/ MONO
I²C BUS DECODER
YUV In
U_CON
V_CO
C_IN
BA7652
WSFI
CFIN
YFIN
FROM FRONT A/V BOARD
Y/C Front In
WSRI
YS_IN
Y/C Rear In
Matrix
From Digital Board
D_R
D_G
D_B
D_CVBS
D_C
D_Y
FRONT END
VFV
Front Cinch In
CVBSFIN
IS1
IS2
Rear Cinch In
i²C

Fig. 6

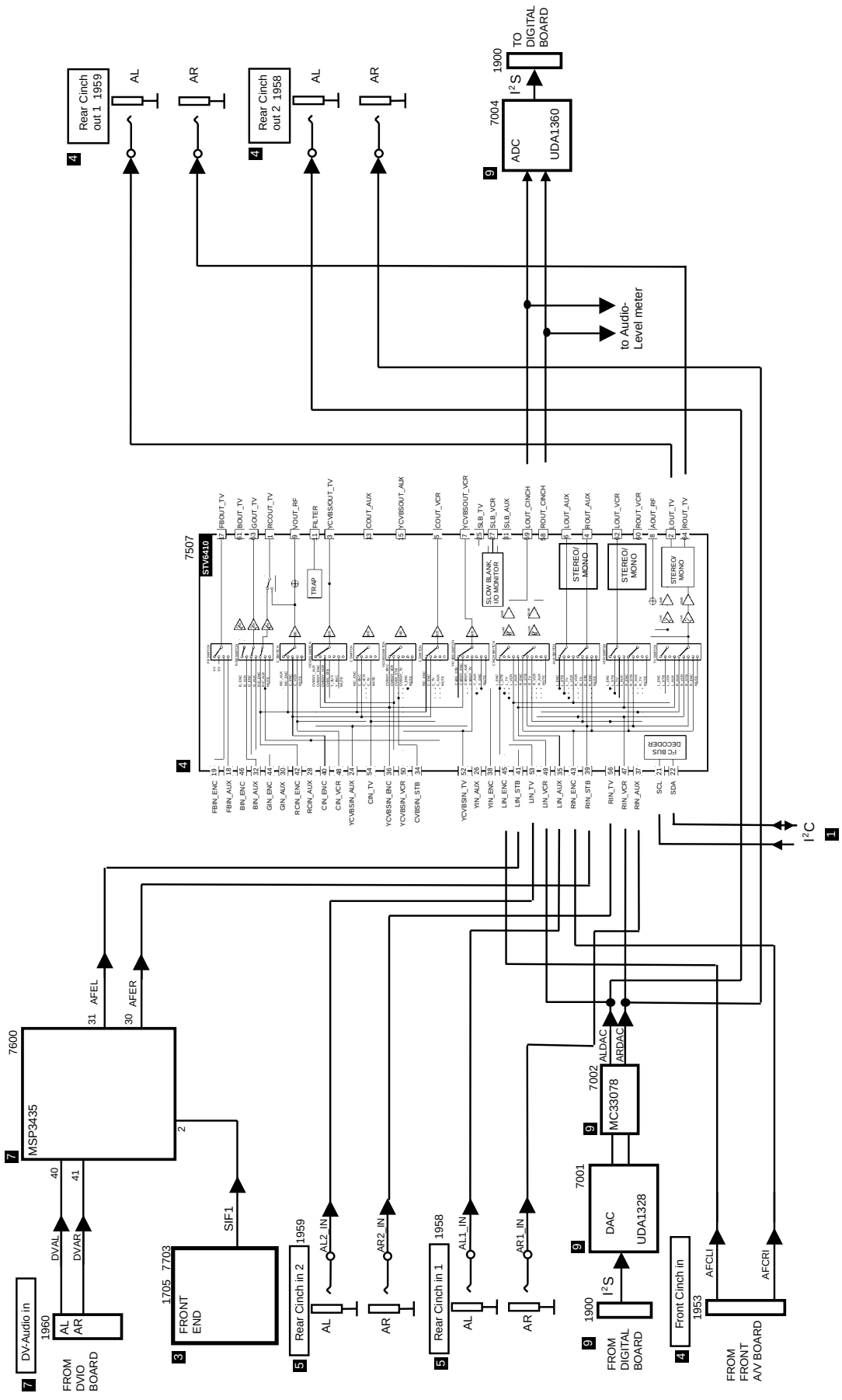

Rear Cinch out 1 1959
Rear Cinch out 2 1958
AL
AR
TO DIGITAL BOARD
1900
I²S
7004
ADC
UDA1360
to Audio-Level meter
7507
STV6410
TRAP
SLOW BLANK, I/O MONITOR
STEREO/ MONO
I²C BUS DECODER
FBIN_ENC
FBIN_AUX
BIN_ENC
BIN_AUX
GIN_ENC
GIN_AUX
RCIN_ENC
RCIN_AUX
CIN_ENC
CIN_VCR
YCVBSIN_AUX
CIN_TV
YCVBSIN_ENC
YCVBSIN_VCR
CVBSIN_STB
YCVBSIN_TV
YIN_AUX
YIN_ENC
LIN_ENC
LIN_STB
LIN_TV
LIN_VCR
LIN_AUX
RIN_ENC
RIN_STB
RIN_TV
RIN_VCR
RIN_AUX
SCL
SDA
FBOUT_TV
BOUT_TV
GOUT_TV
ROUT_TV
VOUT_RF
FILTER
YCVBSOUT_TV
COUT_AUX
YCVBSOUT_AUX
COUT_VCR
YCVBSOUT_VCR
SLB_TV
SLB_VCR
SLB_AUX
LOUT_CINCH
ROUT_CINCH
LOUT_AUX
ROUT_AUX
LOUT_VCR
ROUT_VCR
AOUT_RF
LOUT_TV
ROUT_TV
I²C
7600
MSP3435
AFEL
AFER
DV:Audio in
1960
DVAL
DVAR
FROM DVIO BOARD
1705 7703
FRONT END
SIF1
Rear Cinch in 2
1959
AL2_IN
AR2_IN
Rear Cinch in 1
1958
AL1_IN
AR1_IN
7002
MC33078
ALDAC
ARDAC
7001
DAC
UDA1328
FROM DIGITAL BOARD
Front Cinch in
1953
AFCLI
AFCRI
FROM FRONT A/V BOARD

Fig. 7

5. Digital Board

5.1 Record Mode

Video Part

Analog Video input signals CVBS, YC and UV(RGB for EURO and YUV for USA) are routed via the analog board to connector 1601 and sent to IC7500 SAA7118 (Video Input Processor).
Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1603 and further also to IC7500.
IC7500 (VIP) encodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7403 SAA6752H (EMPRESS) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.
IC7403 (EMPRESS) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio is sent from the analog board to IC7403 EMPRESS via connector 1602. The EMPRESS compresses I2S audio data into an AC3 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, EMPRESS IC7403, MPEG decoder IC7200 (Sti5508) and buffers the data streams that are coming from or going to these hardware modules.
In IC7100 (VSM), the video MPEG2 stream and the audio AC3 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7200 (Sti5508). This IC decodes the MPEG stream into analog video and I2S audio.
The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

5.2 Playback Mode

During playback, the serial data from the Basic Engine is going directly to the Sti5505 via the serial front-end I2S interface.
The Sti5508 is a MPEG & Audio/video decoder and has the following outputs:

- To the analog board:
  – analog video RGB, YC, CVBS
  – I2S audio (PCM format)
  – SPDIF audio (digital audio output)
- To the Progressive scan board:
  – digital video YC(7:0).

5.3 S2B Interface

The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

5.4 System Clock

System clocks(27MHz) of VSM, Sti5508, EMPRESS and Progressive Scan are generated by oscillator 7906

5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7102 (PLL) because then, the audio clock must be sychronized with the incoming video (VIP_FID) from the VIP.
During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7900 (MK2703S). Both ACC_ACLK_OSC(also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock to the STI5508. The EMPRESS IC derives from the incoming ACLK_EMP the I2S audio encoder clocks AE_BCLK and AE_WCLK which are sent to the VSM.

5.6 On/Off

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

5.7 Reset

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

5.8 I2C Bus

Sti5508 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7201 NVRAM
- IC7403 EMPRESS
- IC7500 VIP
- IC7700 FLI2200 Video Deinterlacer Line Doubler
- IC7801 ADV7196 Video Denc

5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7301 and 7302: Flash memories which contain the application and diagnostic software
- IC7100: VSM
- IC7200: MPEG AV Decoder

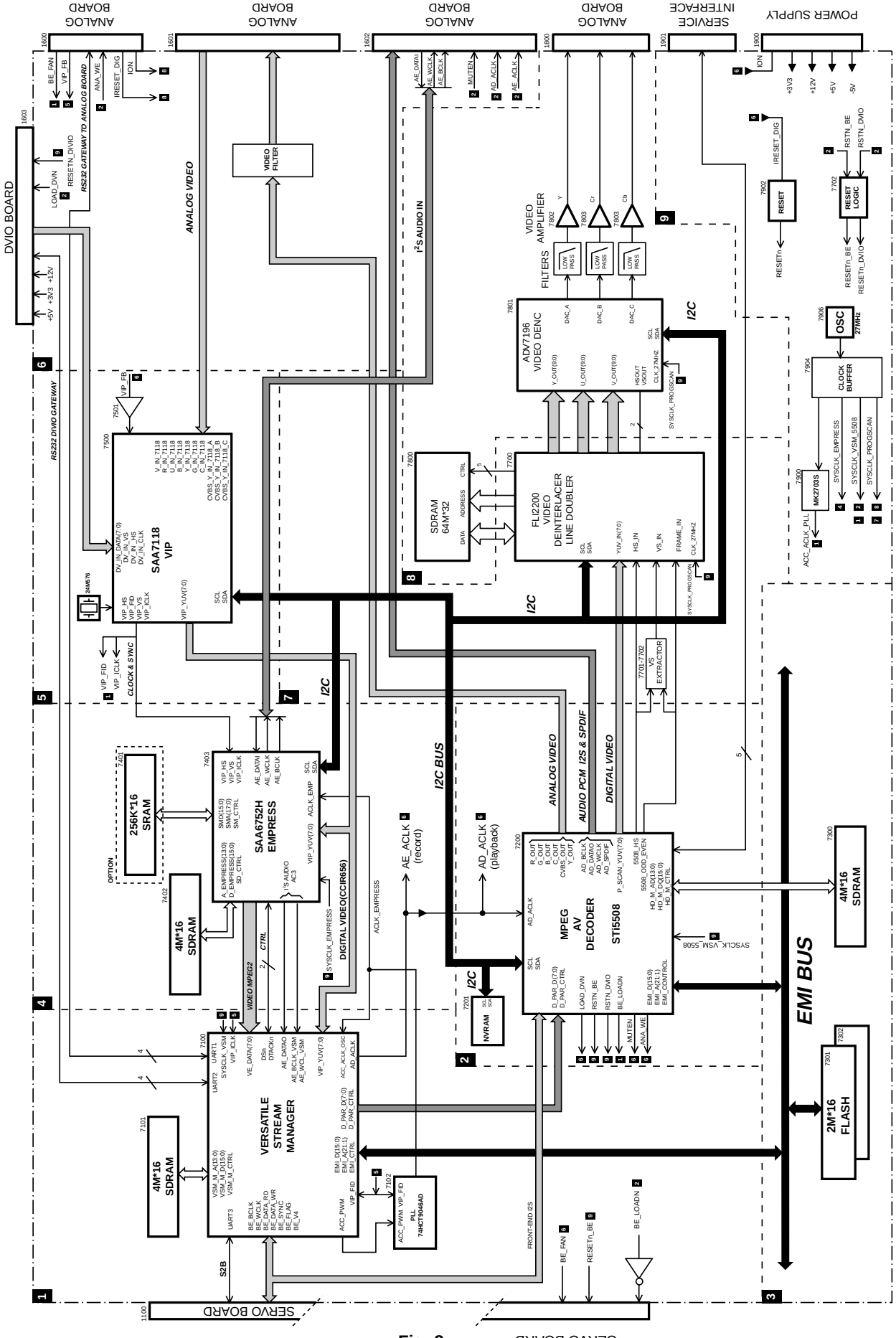

ANALOG BOARD
ANALOG BOARD
ANALOG BOARD
ANALOG BOARD
SERVICE INTERFACE
POWER SUPPLY
DVIO BOARD
ANALOG VIDEO
VIDEO FILTER
I²S AUDIO IN
RS232 GATEWAY TO ANALOG BOARD
RS232 DVIO GATEWAY
VIDEO AMPLIFIER
FILTERS
ADV7196 VIDEO DENC
SAA7118 VIP
SDRAM 64M*32
FLI2200 VIDEO DEINTERLACER LINE DOUBLER
I2C
I2C BUS
CLOCK & SYNC
SAA6752H EMPRESS
256K*16 SRAM
4M*16 SDRAM
VERSATILE STREAM MANAGER
MPEG AV DECODER STi5508
ANALOG VIDEO
AUDIO PCM I2S & SPDIF
DIGITAL VIDEO
EMI BUS
2M*16 FLASH
NVRAM
CLOCK BUFFER
OSC 27MHz
RESET
RESET LOGIC
SERVO BOARD
SERVO BOARD

Fig. 8

5.10 Progressive Scan

Description

The progressive scan part is integrated in the Digital Board and built around the SAGE Fli2200 de-interlacer / line doubler (7701). This I2C controlled de-interlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing).

The de-interlacer gets his digital YUV input data from the STi5508 (7200). The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz.

Because the STi5508 doesn't have a Vsync output the odd/even output of this IC has to be translated to a Vsync signal.

Some glue logic has been added to extract the vertical sync.

The glue logic circuit consists of Flip-Flop IC 74HC74D (7701) and EXOR 74LVC86 (7702). The next diagram shows how the vertical sync is extracted.

Vertical Sync

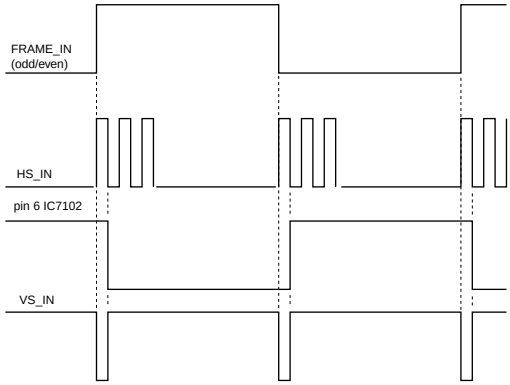


Fig. 9

The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices ADV71967 MacroVision compliant DENC (7801).

The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7802-7803).

The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.

6. Divio Board

6.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. Input is a stream from a DV-camcorder IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present.

The following picture shows the location of the DVIO Module inside the DVDR set.

Description DIVIO Module

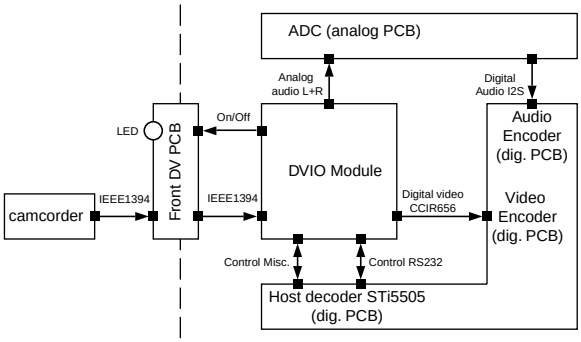


Fig. 10

6.2 Block Diagram

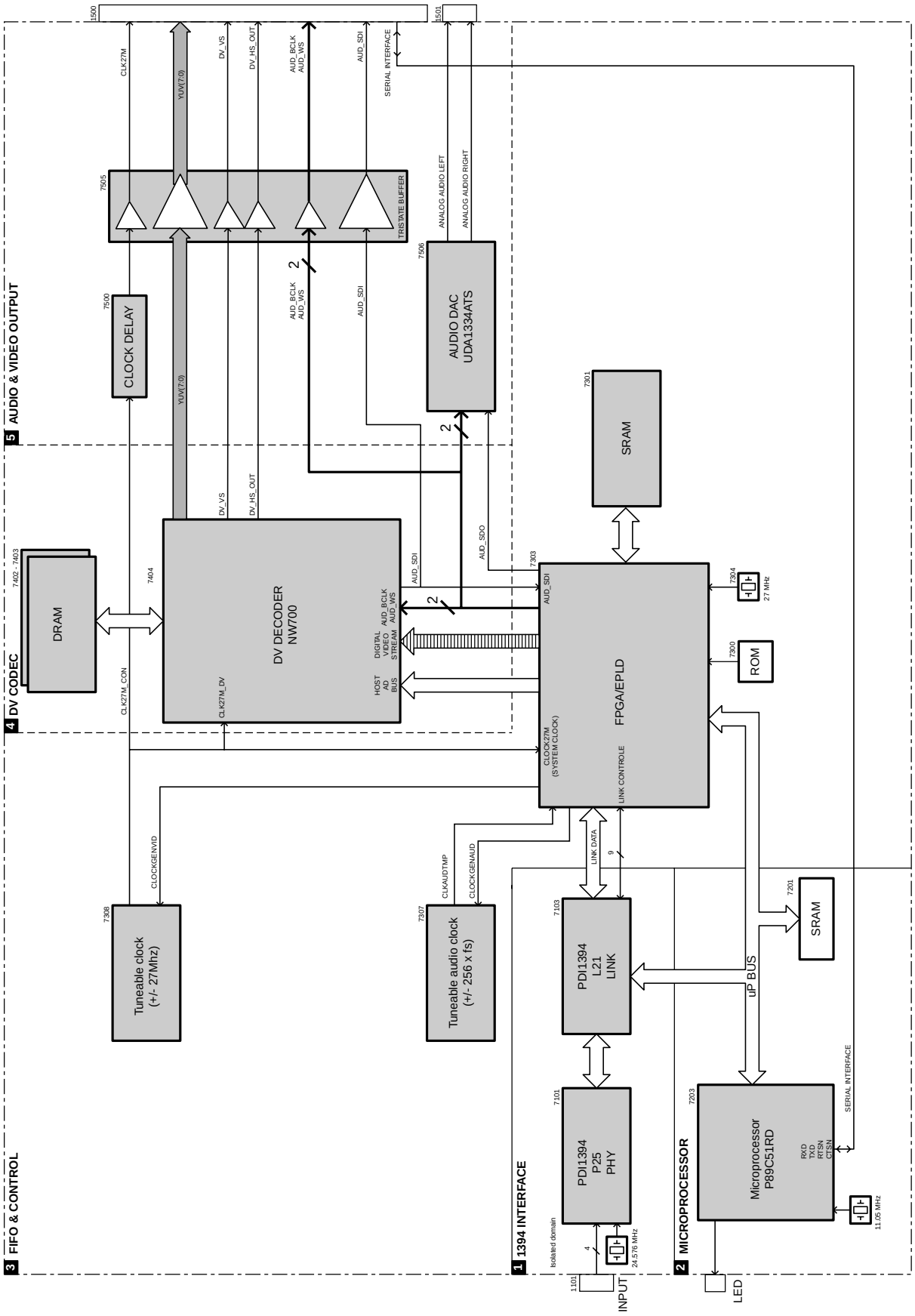


Fig. 11

6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
   - PDI1394P25(7101)
   - PDI1394L40(7103)
2. Micro-controller
   - 89C51RD2(7203)
   - 32kb SRAM(7201)
3. FIFO and Control
   - FPGA/EPLD(7303)
   - SRAM(7301)
   - Clock generation(7307, 7308)

   – Independently tuneable audio and video clock, implemented with FPGA and PLL
4. DV-Decoder
   - NW700(7404)
   - EDO DRAM(7402, 7403)
5. Audio & Video output
   - Audio DAC UDA1334ATS(7602)
   - Clock delay(7500)
   - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a PDI1394P25 physical layer and a PDI1394L40 link layer.
It has the following features:

- S200 operation (200 megabit per second)
- One i.Link port (4 pin)
- AV link port

Micro-Controller

The 89C51RD2 processor has a 8051 cpu with the following extra features:

- 64 kilobyte of flash memory as program memory
- 1 kilobyte of internal data memory
- watchdog timer
- PCA outputs
- Power control modes
- Speed allowed up to 33 MHz but used at 11.0592 MHz
- On board ISP(In Circuit Programming) functionality

ISP

By use of In Circuit Programming, it is possible to update the software of the DVIO board that is in the 89C51RD2. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. A programming voltage of 5V is always present at the Vpp pin. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Fifo and Control

In decode mode, an isochronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a FIFO buffer (ping-pong buffer type, i.e. 2 buffers that can hold one whole frame each).

Reset

The FPGA controls the reset signals on the board. This has the advantage that it is possible to reset the board both from software and hardware.

Reset

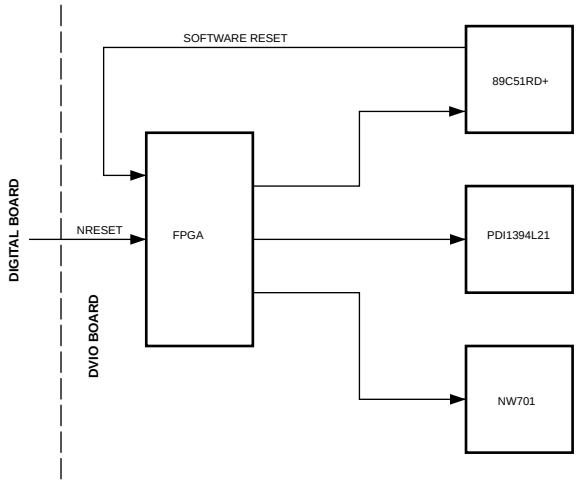


Fig. 12

The board reset NRESET will reset the whole board, and the software reset can reset everything except the microprocessor itself. Power-on reset is implemented by adding pull-ups and pull-downs to the reset inputs of the devices. Since the FPGA will tri-state all the pins during configuration, reset is active during configuration time. After configuration of the FPGA, the reset signals are driven inactive. The NRESET signal is used to reset the DVIO board. After reset, the tri-state buffers to connector 1500 are disabled.

Clock Circuit

There are 2 clocks to consider in the system, this is the video clock and the audio clock. These two clocks do not have a relation, so these clocks must be considered independently.
The video clock is approximately 27 MHz. When data is flowing from an external source that is supposed to have the same frequency, it does not have exactly the same clock. Because of this, buffers may under-run of over-run. Since the clock can not be directly recovered from the 1394 interface, there has to be another solution. This solution is a tuneable clock that is adjusted to the required frequency to process at the rate of the incoming data.
The hardware implementation of such a tuneable clock is as follows:

Clock Circuit

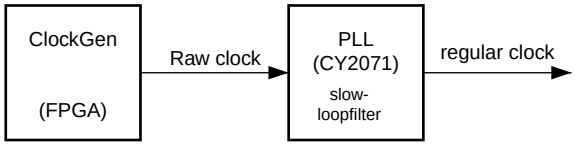


Fig. 13

The same can be applied for the audio clock. For this clock, a frequency of 8.192 MHz, 11.2896 MHz or 12.228 MHz is required. This depends on the sample-rate frequency(32kHZ, 44.1kHZ or 48kHZ)of the audio signal.

DV Decoder

The AV-data will go from the FIFO to the NW700. The NW700 decodes the stream into video data in 656 format and audio data in I2S format.
The microprocessor has the ability to read the status registers of the NW700 through the FPGA. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Audio & Video Output

The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board.
The tristate buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.
The clock delay synchronizes the AV clock with the AV data at the output.

■ ABBREVIATION LIST

Digital Board

+12V
+12V Power Supply
+2V5_FLI
+2V5 Power Supply for FLI
+2V5_PLL
+2V5 Power Supply for PLL
+3V3
+3V3 Power Supply
+3V3_ANA
+3V3 Power Supply Analogue
+3V3_DD
+3V3 Power Supply Digital
+3V3_FLI
+3V3 Power Supply for FLI
+5V
+5V Power Supply
+5V_BUFFER
+5V Power Supply for Video Filters
5508_HS
Horizontal Synchronisation from Host Decoder to Progressive Scan
5508_ODD_EVEN
Odd - Even control from Host Decoder to Progressive Scan
-5V
-5V Power Supply
-5V_BUFFER
-5V Power Supply for Video Filters
A_EMPRESS(13:0)
EMPRESS address output to SDRAM
ACC_ACLK_OSC
Audio Clock PLL output sync with incoming video for record
ACC_ACLK_PLL
Audio Clock PLL output for play back
ACLK_EMP
EMPRESS audio clock output
AD_ACLK
Audio Decoder Clock
AD_BCLK
Audio Decoder I2S bit clock
AD_DATAO
Audio Decoder Output data (PCM)
AD_SPDIF33
Audio digital output to the analog board
AD_WCLK
Audio Decoder I2S word clock
AE_ACLK
Audio Encoder Clock
AE_ACLK_OEN
Audio Encoder Clock Output Enable
AE_BCLK
Audio Encoder I2S bit clock
AE_BCLK_DV
Audio Encoder I2S bit clock to DVIO
AE_BCLK_VSM
Audio Encoder I2S bit clock to VSM
AE_DATAI
Audio Encoder Input data (PCM)
AE_DATAI_DV
Audio Encoder Input data (PCM) from DVIO
AE_DATAO
Audio Encoder Output data (PCM)
AE_WCLK
Audio Encoder I2S word clock
AE_WCLK_DV
Audio Encoder I2S word clock to DVIO
AE_WCLK_VSM
Audio Encoder I2S word clock to VSM
ANA_WE
Analogue write enable
ANA_WE_LV
Analogue write enable Low Voltage
B_IN_VIP
Video blue input to Video Input Processor
B_OUT
Video blue output from Host Decoder
B_OUT_B
Filtered blue video output
BA
Bank Address
BCLK_CTL_SERVICE
Bitclock control Service Interface
BE_BCLK
Basic Engine I2S bit clock
BE_BCLK_VSM
Basic Engine I2S bit clock to VSM
BE_CPR
Basic Engine Control Processor ready to accept data
BE_DATA_RD
Basic Engine Data read
BE_DATA_WR
Basic Engine Data write
BE_FAN
Basic Engine FAN
BE_FLAG
Basic Engine error flag
BE_IRQN
Basic Engine interrupt request
BE_LOADN
Basic Engine LOAD(LOW active)
BE_RXD
Basic Engine S2B received data
BE_SUR
Basic Engine servo unit ready to accept data (S2B)
BE_SYNC
Basic Engine sector/abs time sync
BE_TXD
Basic Engine S2B transmitted data
BE_V4
Basic Engine versatile input pin

BE_WCLK
Basic Engine I2S word clock
C_IN
Video Chrominance input
C_IN_VIP
Chrominance input to Video Input Processor
C_OUT
Chrominance output from Host Decoder
C_OUT_B
Filtered Chrominance output
CAS
Column Address strobe
CB_OUT(9:0)
Chrominance Blue out
CLK4
SDRAM clock
CPUINT0
Control processor unit interrupt
CPUINT1
Control processor unit interrupt
CR_OUT(9:0)
Chrominance Red out
CTS1P
Clear to send (Service Interface)
CVBS_OUT
Composite video output out of the Host Decoder
CVBS_OUT_B
Filtered Composite video output
CVBS_OUT_B_VIP
Composite video output to Video Input Processor(digital board
video loop)
CVBS_Y_IN
Composite video/Luminance input
CVBS_Y_IN_A
Composite video/Luminance input to Video Input Processor
CVBS_Y_IN_B
Composite video/Luminance input to Video Input Processor
CVBS_Y_IN_C
Composite video/Luminance input to Video Input Processor
D_ADDR(10:0)
Address bus
D_DATA(29:0)
Data bus
D_EMPRESS(15:0)
SDRAM data input/output of EMPRESS
D_PAR_D(7:0)
Front-end parallel interface data (record)
D_PAR_DVALID
Front-end parallel interface data valid
D_PAR_REQ
Front-end parallel interface request
D_PAR_STR
Front-end parallel interface strobe
D_PAR_SYNC
Front-end parallel interface sync
DV_IN_CLK
Digital Video in clock from DVIO board
DV_IN_DATA(7:0)
Digital Video in data bus from DVIO board
DV_IN_HS
Digital Video in horizontal synchronisation from DVIO board
DV_IN_VS
Digital Video in vertical synchronisation from DVIO board
EMI_A(21:1)
External Memory Interface Address Bus(Host Decoder)
EMI_BE0N
External Memory Interface Lower byte enable(Host Decoder)
EMI_BE1N
External Memory Interface Upper byte enable(Host Decoder)
EMI_CAS0N
External Memory Interface SDRAM column address strobe(Host Decoder)
EMI_CE1N
External Memory Interface VSM Lower bank enable
EMI_CE2N
External Memory Interface VSM Higher bank enable
EMI_CE3N
External Memory Interface flash IC's enable
EMI_D(15:0)
External Memory Interface Data Bus(Host Decoder)
EMI_PROCCLK
External Memory Interface Processor Clock(Host Decoder)
EMI_RWN
External Memory Interface Read/Write control signal(Host Decoder)
EMI_WAIT
External Memory Interface Wait state request(Host Decoder)
EMPRESS_BOOT
EMPRESS BOOT select input
EMPRESS_IRQN
EMPRESS Interrupt request output
FLASH_OEN
FLASH output enable control signal
G_IN_VIP
Video green input to Video Input Processor
G_OUT
Video green output from Host Decoder
G_OUT_B
Filtered green video output from Host Decoder
GNDD
Digital Ground
HD_M_AD(13:0)
Host Decoder SDRAM address bus
HD_M_CASN
Host Decoder SDRAM column address strobe
HD_M_CLK
Host Decoder SDRAM clock
HD_M_CS0N
Host Decoder SDRAM chip select

HD_M_DQ(15:0)
Host Decoder SDRAM data bus
HD_M_DQML
Host Decoder SDRAM data mask enable(Lower)
HD_M_DQMU
Host Decoder SDRAM data mask enable(Upper)
HD_M_RASN
Host Decoder SDRAM row address strobe
HD_M_WEN
Host Decoder SDRAM write enable
HSOUT
Horizontal synchronisation OUT
ION
Inverted ON: Enable the power supply for the digital board when LOW
IRESET_DIG
Initialisation of the digital board, HIGH when power ON
JTAG3_TCK
JTAG Test Clock
JTAG3_TD_VIP_TO_VE
JTAG Transmitted Data Video Input Processor to Video Encoder
JTAG3_TD_VSM_TO_VIP
JTAG Transmitted Data Versatile Stream Manager to Video
Input Processor
JTAG3_TMS
JTAG Test Mode Select
JTAG3_TRSTN
JTAG Test part ResetN
LOAD_DVN
LOAD Digital Video(LOW active)
MUTEN
Mute enable
MUTEN_LV
Mute enable Low Voltage
P_SCAN_YUV(7:0)
Progressive Scan digital video bus
R_IN_VIP
Video Red input to Video Input Processor
R_OUT
Video Red output from Host Decoder
R_OUT_B
Filtered Red Video output from Host Decoder
RAS
Row Address Strobe
RESETN
Reset Host Decoder
RESETN_BE
System reset basic engine (buffered)
RESETN_DVIO
System reset Digital Video Input Output (buffered)
RESETN_VE
System reset Video Encoder
ROMH_CEN
Flash 2 chip enable
ROML_CEN
Flash 1 chip enable
RSTN_BE
Reset control of basic engine
RSTN_DVIO
Reset control of DVIO
RTS1P
Ready To Send data to service serial interface
RX1P
Receive data from service serial interface
SCL
I2C bus clock
SD_CASN
SDRAM Column Address strobe output (active LOW)
SD_CLK
SDRAM clock output
SD_CLKE
SDRAM clock enable output
SD_CSN
SDRAM
SD_DQM(1:0)
SDRAM data mask enable output
SD_RASN
SDRAM row address strobe output
SD_WEN
SDRAM write enable output
SDA
I2C bus data
SEL_ACLK1
Select audio clock(playback)
SM_CS3N
SRAM chip select
SM_LBN
SRAM lower bank
SM_OEN
SRAM output enable
SM_UBN
SRAM upper bank
SM_WEN
SRAM write enable
SMA(17:0)
SRAM address output
SMD(15:0)
SRAM data input/output
SYSCLK_EMPRESS
System clock EMPRESS
SYSCLK_PROGSCAN
System clock Progressive Scan
SYSCLK_VSM_5508
System clock VSM and Host decoder
TX1P
Transmit data to service serial interface
U_IN
Video U input
U_IN_VIP
Video U input to Video Input Processor
V_IN
Video V input
V_IN_VIP
Video V input to Video Input Processor

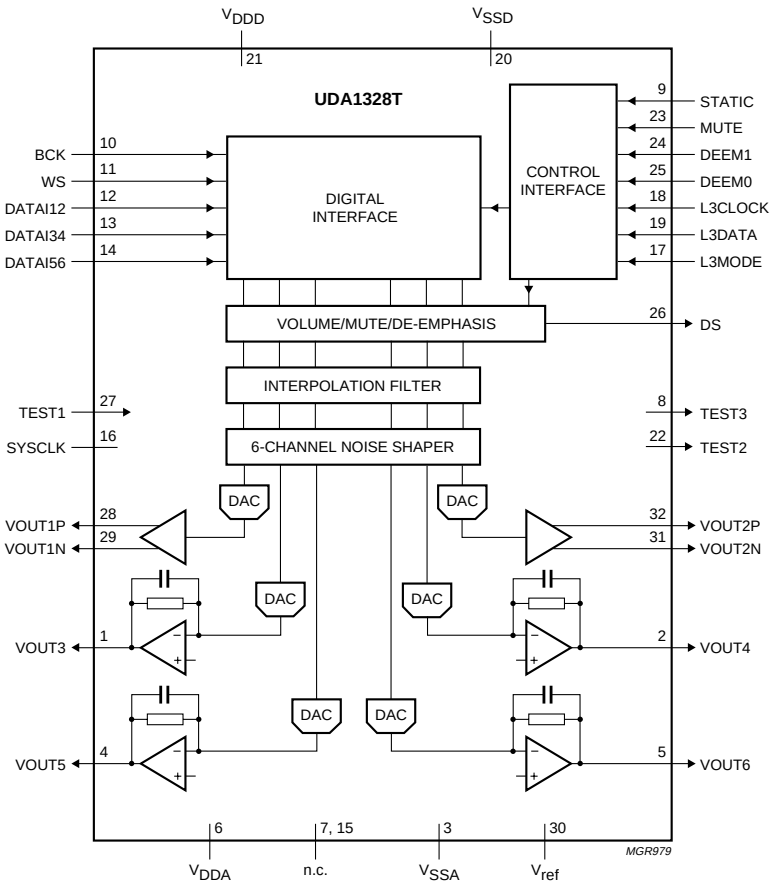
VCC3_CLK_BUF
Power supply 3V3 clock buffer
VCC3_VSM
Power supply 3V3 Versatile Stream Manager
VCC3_VSM_MEM
Power supply 3V3 Versatile Stream Manager Memory
VCC5_4046
Power supply 5V to PLL IC
VDD_125
Power supply 5V to buffer 7202
VDD_CORE
Sti5508 Core supply voltage 2.5V
VDD_EMP
Empress supply voltage 3.3V
VDD_EMP_CORE
Empress Core supply voltage 2.5V
VDD_FLASH_H
Flash 7301 supply voltage
VDD_FLASH_L
Flash 7302 supply voltage
VDD_LVC32
Power supply LVC32
VDD_PCM
Power supply Audio decoder of Sti5508
VDD_PLL
Power supply PLL audio decoder of Sti5508
VDD_RGB
Power supply video encoder of Sti5508
VDD_STI
Power supply of Sti5508
VDD_YCC
Power supply video encoder of Sti5508
VDD5_MK2703
Power supply MK2703
VDD5_OSC
Power supply Oscillator
VDDA1A_7118
Power supply for analog input of VIP
VDDA2A_7118
Power supply for analog input of VIP
VDDA3A_7118
Power supply for analog input of VIP
VDDA4A_7118
Power supply for analog input of VIP
VDDE_7118
Power supply digital for peripheral cells of VIP
VDDI_7118
Power supply digital for core of VIP
VDDX_7118
Power supply for crystal oscillator of VIP
VE_DATA(7:0)
Video Encoder data Bus
VE_DSN
Video Encoder Data Strobe
VE_DTACKN
Video Encoder Data Transfer acknowledge
VIP_ERROR
Video Input Processor error
VIP_FB
Video Input Processor Fast Blanking
VIP_FID_FF
Video Input Processor field indentifier to Flip Flop
VIP_HS
Video Input Processor horizontal synchronisation
VIP_ICLK
Video Input Processor input Clock
VIP_IDQ
Video Input Processor output data qualifier
VIP_IGP1
Video Input Processor input general purpose 1
VIP_INT
Video Input Processor interrupt
VIP_RTS1
Video Input Processor ready to send
VIP_VS
Video Input Processor vertical synchronisation
VIP_YUV(7:0)
Video Input Processor digital video(CCIR 656)
VS_IN
Vertical synchronisation IN
VSM_M_A(13:0)
Versatile Stream Manager SDRAM address bus
VSM_M_CASN
Versatile Stream Manager SDRAM column address strobe
VSM_M_CLKEN
Versatile Stream Manager SDRAM clock enable
VSM_M_CLKOUT
Versatile Stream Manager SDRAM clock out
VSM_M_D(15:0)
Versatile Stream Manager SDRAM data bus
VSM_M_LDQM
Versatile Stream Manager SDRAM lower data mask enable
VSM_M_RASN
Versatile Stream Manager SDRAM row address strobe
VSM_M_UDQM
Versatile Stream Manager SDRAM upper data mask enable
VSM_M_WEN
Versatile Stream Manager SDRAM write enable
VSM_UART1_CTSN
Versatile Stream Manager UART1 clear to send to analog board (UART1 is gateway to analog board)
VSM_UART1_RTSN
Versatile Stream Manager UART2 clear to send to DVIO board
(UART2 is gateway to DIVIO board)
VSM_UART1_RX
Versatile Stream Manager UART1 ready to send to analog board
VSM_UART1_TX
Versatile Stream Manager UART2 ready to send to DVIO board
VSM_UART2_CTSN
Versatile Stream Manager UART1 received data to analog board

VSM_UART2_RTSN
Versatile Stream Manager UART2 received data to DVIO board
VSM_UART2_RX
Versatile Stream Manager UART1 transmitted data to analog board
VSM_UART2_TX
Versatile Stream Manager UART2 transmitted data to DVIO board
VSOUT
Vertical synchronisation OUT
WE
Write Enable
Y_IN
Luminance input from analog board
Y_OUT
Luminance output from Host Decoder
Y_OUT_B
Filtered luminance output
YY_OUT(9:0)
Luminance output from FLI
Divio Board
+35V_DV_EDO
+3V3 Power supply EDO Bus IC7404
+3V3
+3V3 Power supply
+3V3_DLY
+3V3 Power supply for IC7500
+3V3_DV
+3V3 Power supply for IC7404
+3V3_FPGA
+3V3 Internal Power supply for IC7303
+3V3_FPGA_CONF
+3V3 Power supply for IC 7300
+3V3_IEEE_A
+3V3 Analogue Power supply for PHY IC 7101
+3V3_IEEE_D
+3V3 Digital Power supply for PHY IC 7101
+3V3_IEEE_PLL
+3V3 PLL Power supply for PHY IC 7101
+3V3_LINK
+3V3 Power supply IC7103
+3V3_PLL
+3V3 Power supply IC7307 & IC7308
+3V3_SRAM
+3V3 Power supply IC7301, IC7302, IC7305 & IC7306
+5V
+5V Power supply
+5V_PROC
+5V Power supply IC7200, IC7201, IC7203 & IC7208
+VCC_DV_RAM
+3V3 Power supply for DV_RAM (IC7400--> IC7404)
1394_RSTN
Reset of LINK IC (7103) and PHY IC (7101)
A(0:8)
Address lines
AUD_BCLK
Audio Bit Clock
AUD_MUTE
Audio Mute
AUD_SDI
Audio Serial Data Input
AUD_SDO_CON
Audio Serial Data Output to buffer IC 7505
AUD_SDO_DAC
Audio Serial Data Output to DAC IC 7506
AUD_WS_701
Audio Word Select to DV CODEC IC 7404
AUD_WS_OUT
Audio Word Select to buffer IC 7505
BUFENN_AUD
Buffer Enable Audio
BUFENN_VID
Buffer Enable Video
CCLK
Configuration Clock
CLK27M
27MHz Clock
CLK27M_CON
27MHz Clock to Digital Board
CLK27M_DV
27MHz Clock Digital Video Codec
CLK27M_OSC
27MHz Clock IC7304
CLOCKGENAUD
Clock generator Audio
CLOCKGENVID
Clock generator Video
CTSN
Clear to Send
DATA
Data from config ROM
DONE
Indication of the completion of the configuration process
DOUT
Serial configuration data output
DV_ASN
DVCODEC Address Strobe
DV_DRQN
DVCODEC Data Request Interrupt
DV_DSLN
DVCODEC Data Strobe Lower 8 bits
DV_DSUN
DVCODEC Data Strobe Upper 8 Bits
DV_DTACKN
DVCODEC Data Transfer Acknowledge
DV_ERRN
DVCODEC Error Interrupt
DV_HS_IN
DVCODEC Horizontal synchronisation In
DV_HS_OUT
DVCODEC Horizontal synchronisation Out
DV_LCN
DVCODEC Last Code Interrupt

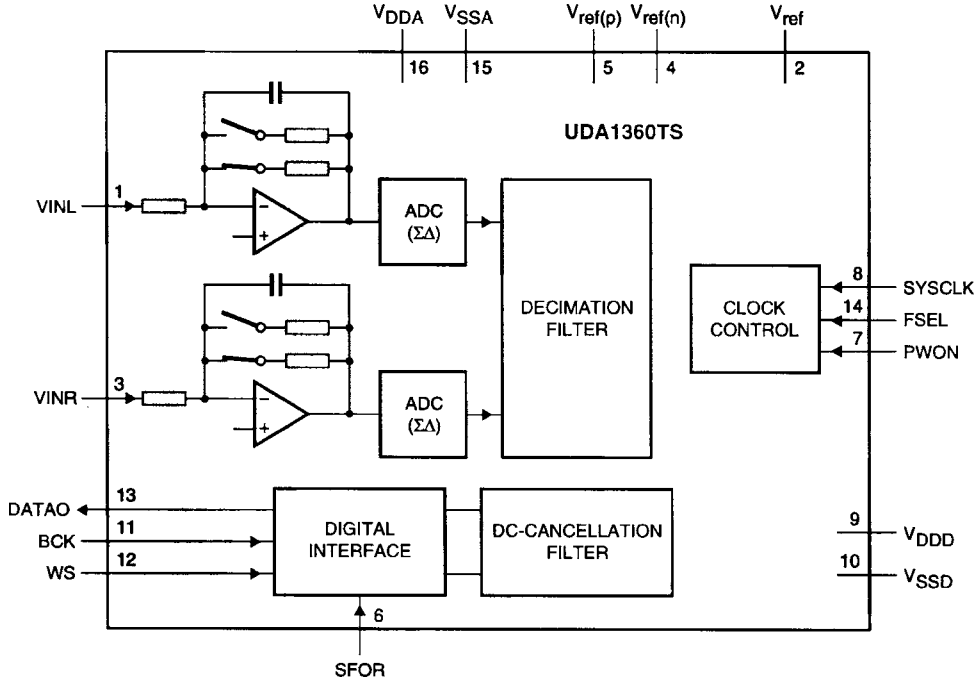
DV_PDN
DVCODEC Power Down
DV_RSTN
DVCODEC System Reset for NW701
DV_RWN
DVCODEC Read/Write control signal
DV_VS
DVCODEC Vertical synchronisation
FIFOA_A(0:15)
FIFO buffer A Address bus
FIFOA_OEN
FIFO buffer A Output enable
FIFOA_WEN
FIFO buffer A Write enable
HAD(0:7)
Host Address/Data bus for register settings of IC7404
INITN
Initiate Configuration
IO(0:30)
Data bus of IC7404
ISPN
In System Program Line (used for programming IC7203)
LCASN
Lower Column Address strobe for IC7404 DRAMS
LINK_AVCLK
LINK IC Audio/Video Interface Clock
LINK_AVFSYNC
LINK IC Audio/Video frame sync
LINK_AVREADY
LINK IC Audio/Video data ready to send
LINK_AVSYNC
LINK IC Audio/Video packet sync
LINK_AVVALID
LINK IC Audio/Video data valid
LINK_CSN
LINK IC chip select
LINK_INTN
LINK IC interrupt
LINKFIFO_DQ(0:7)
Audio Video data interface
PA(0:15)
SRAM processor address
PAD(0:7)
SRAM processor data
PALE
Processor Address Latch Enable
PHY_CNA
PHY 1394 cable not active
PHY_LPS
LINK IC power status
PINT0N
Processor interrupt 0
PINT1N
Processor interrupt 1
PRDN
Processor read
PROGRAMN
Low active input to initiate a configuration cycle
PRSTN
Processor reset
PWRN
Processor write
RASN
Row address strobe
RESETN
DVIO board reset
RTSN
System Reset
RXD
Receive Data
SRAMCE0N
SRAM processor chip enable 0
SRAMRDN
SRAM processor output enable
TCK
Boundary scan Test Clock
TDI
Boundary scan Test Data Input
TDO
Boundary scan Test Data Output
TDO_CONF
Boundary scan Test Data Output from IC 7309
TMS
Boundary scan Test Mode Select
TXD
Transmitted Data
UCASN
Upper column address strobe
WEN
Write Enable control signal to SRAM
YUV(0:7)
Digital Video

■ IC DATA

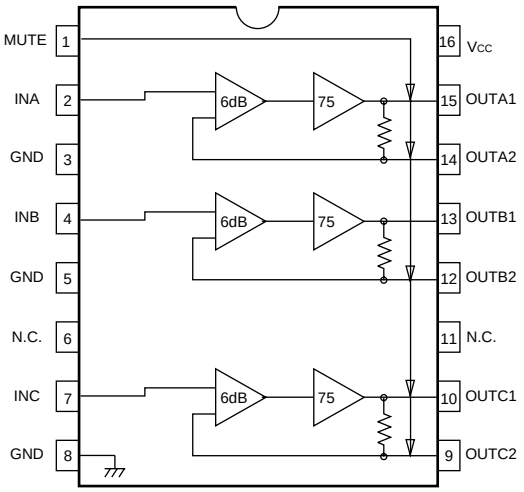
UDA1328T: IC7001



UDA1360TS: IC7004

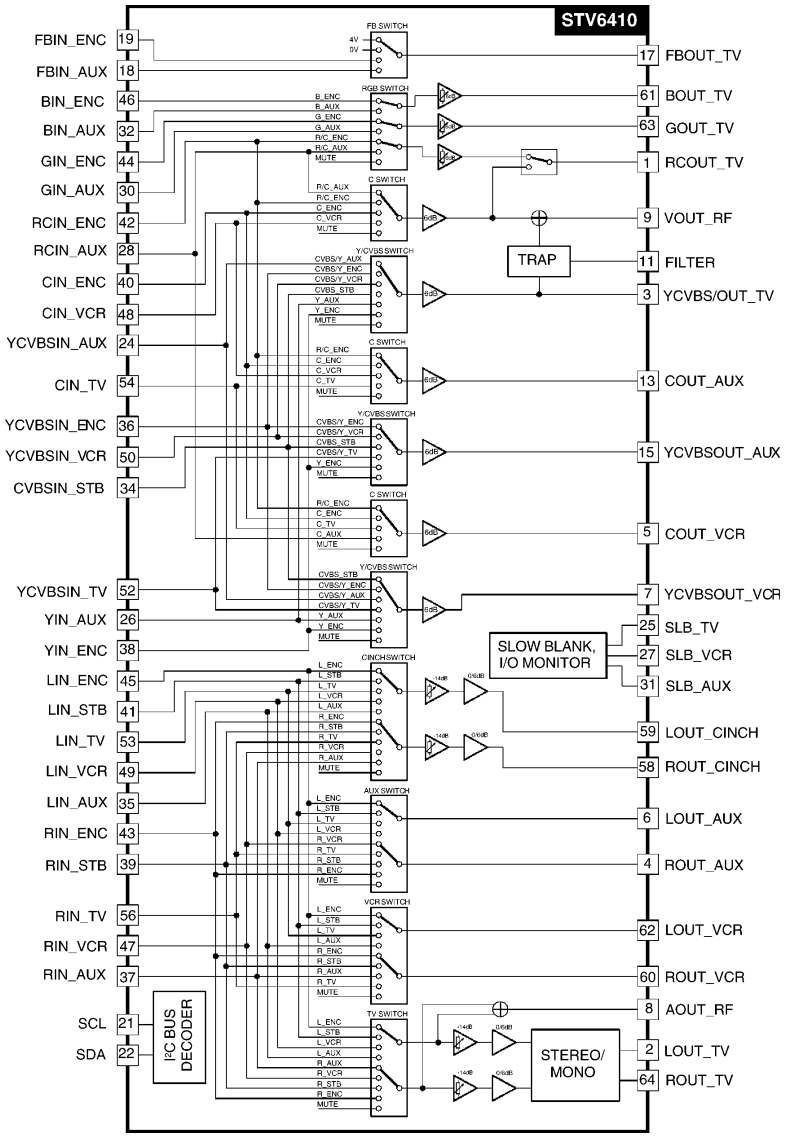


BA7660FS: IC7430

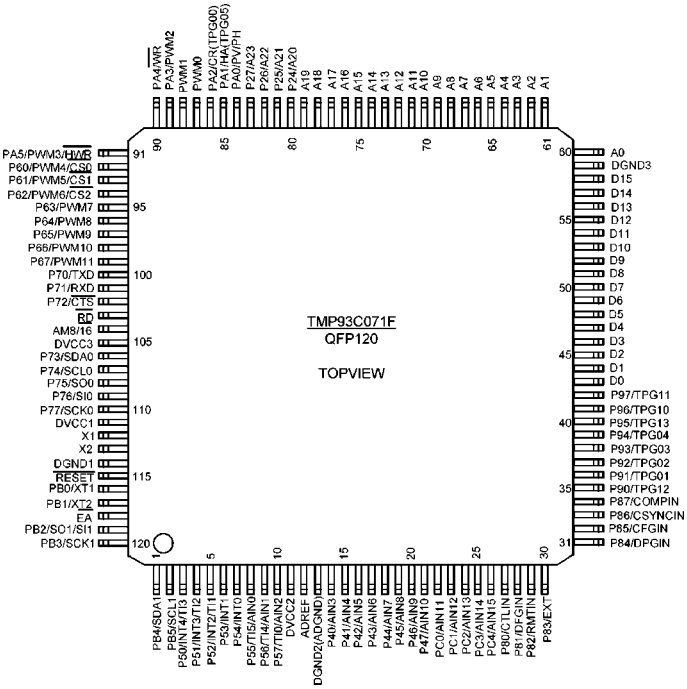


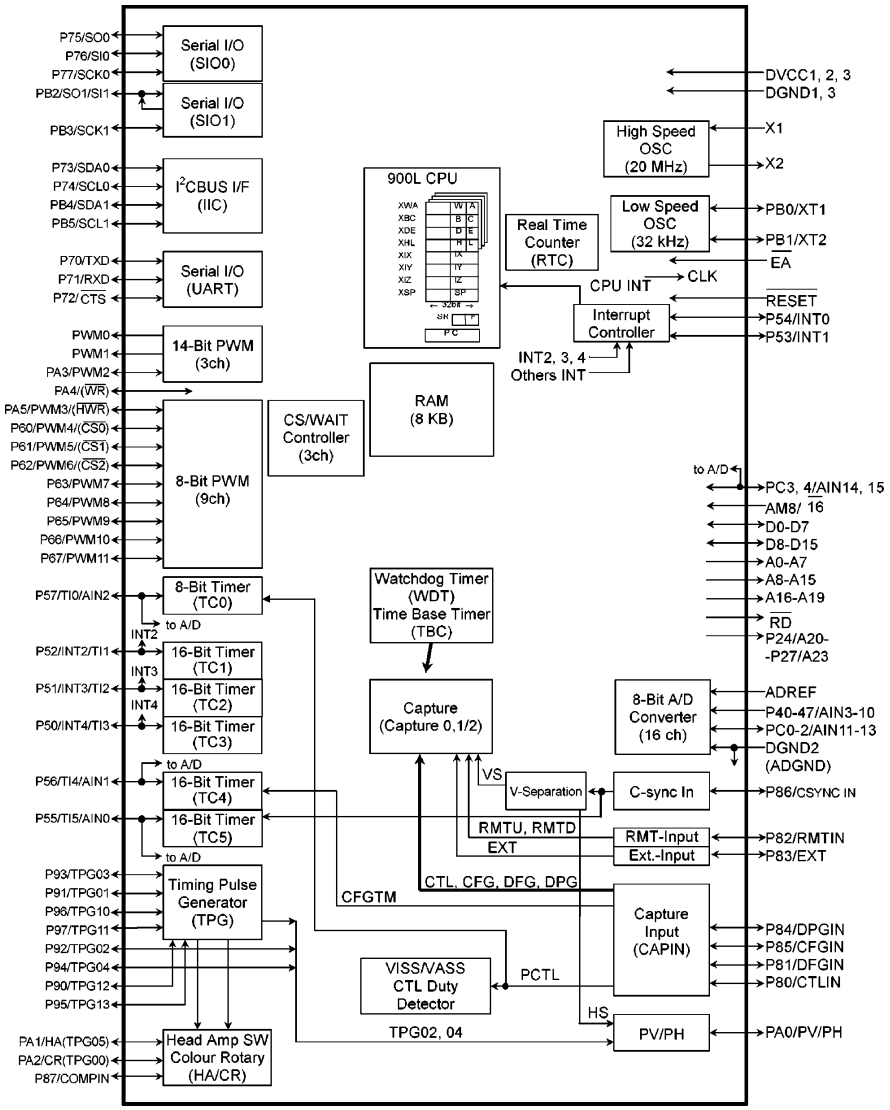
MUTE (1pin)	
H	3ch MUTE
L	NORMAL

STV6410: IC7507

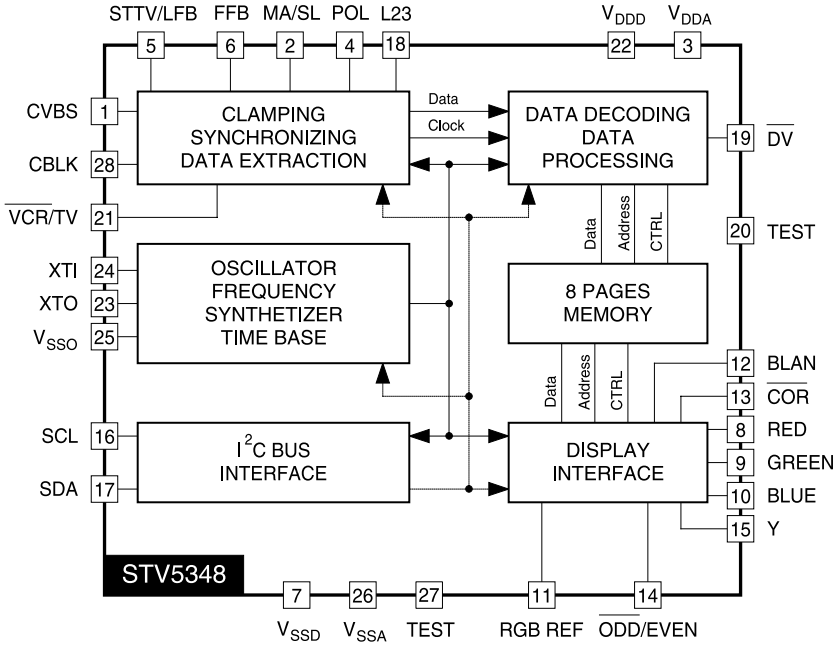


TMP93C071: IC7803

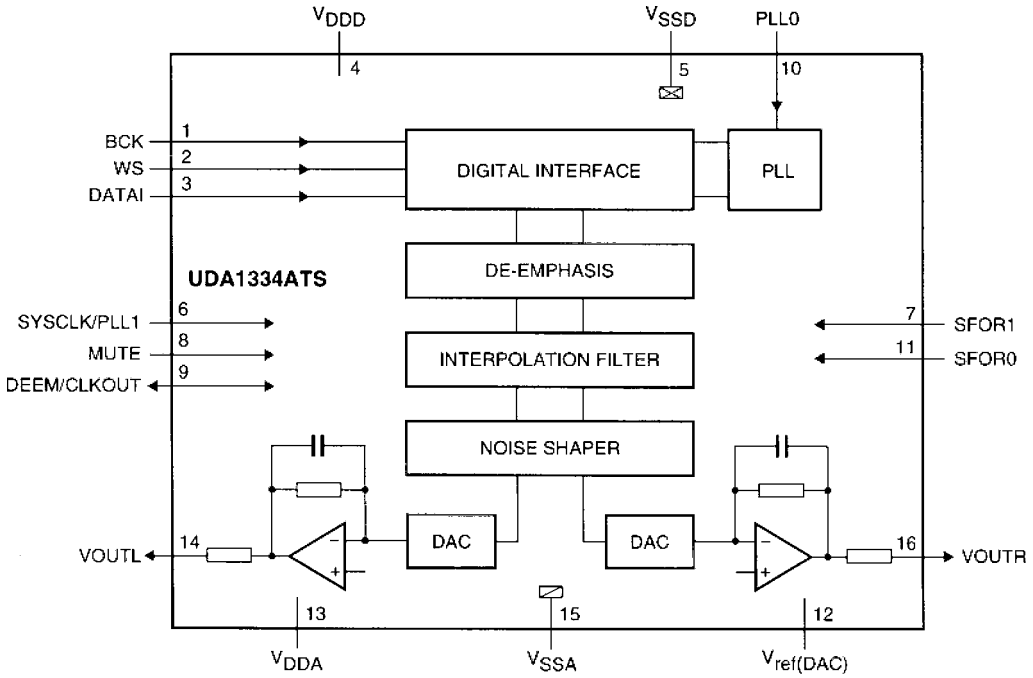




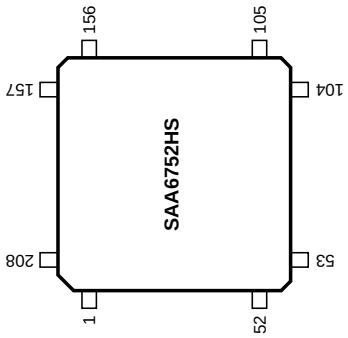
STV5348: IC7990

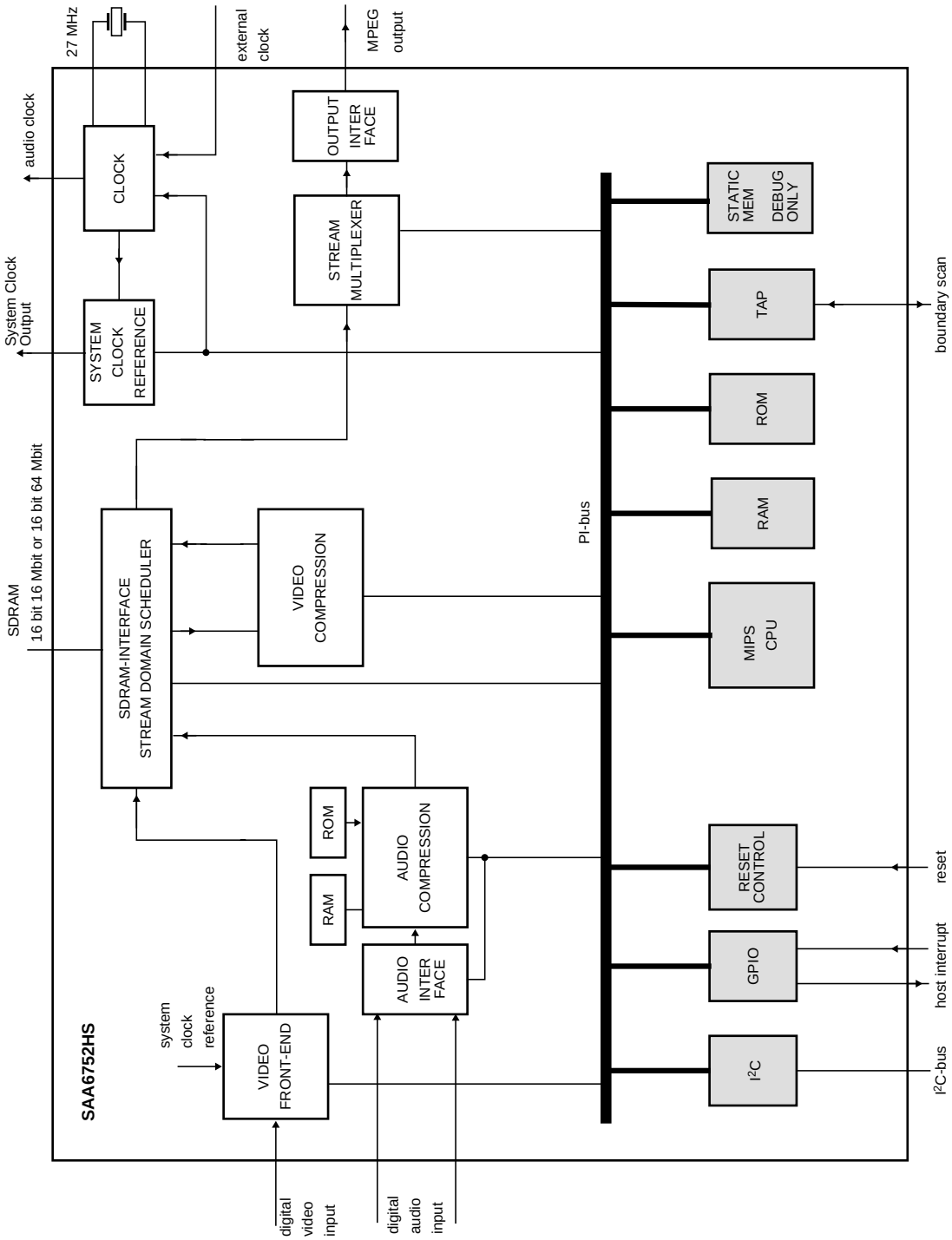


UDA1334TS: IC7506

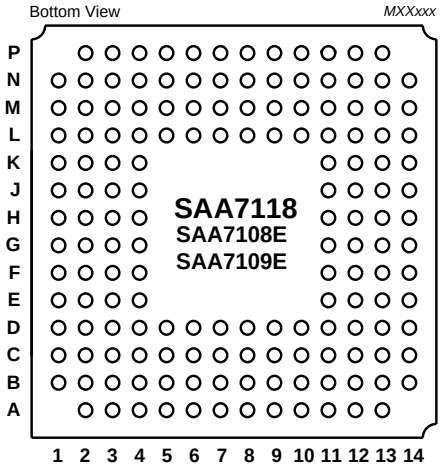


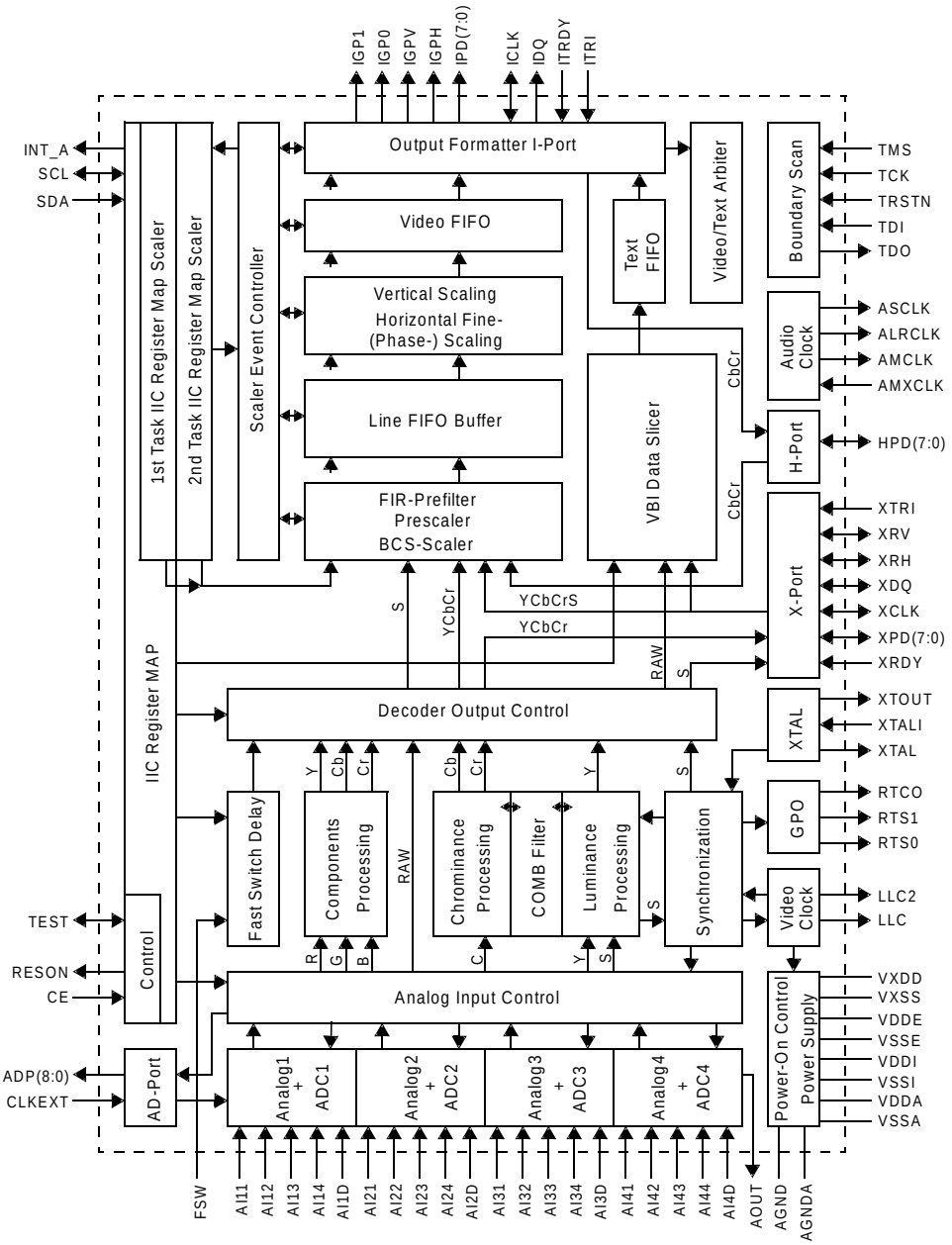
SAA6752HS: IC7403



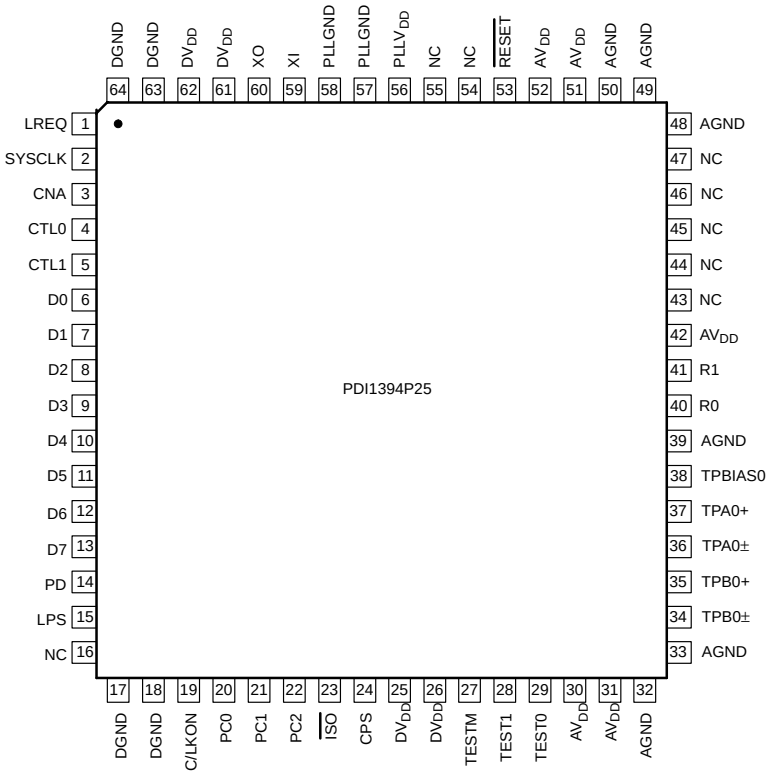


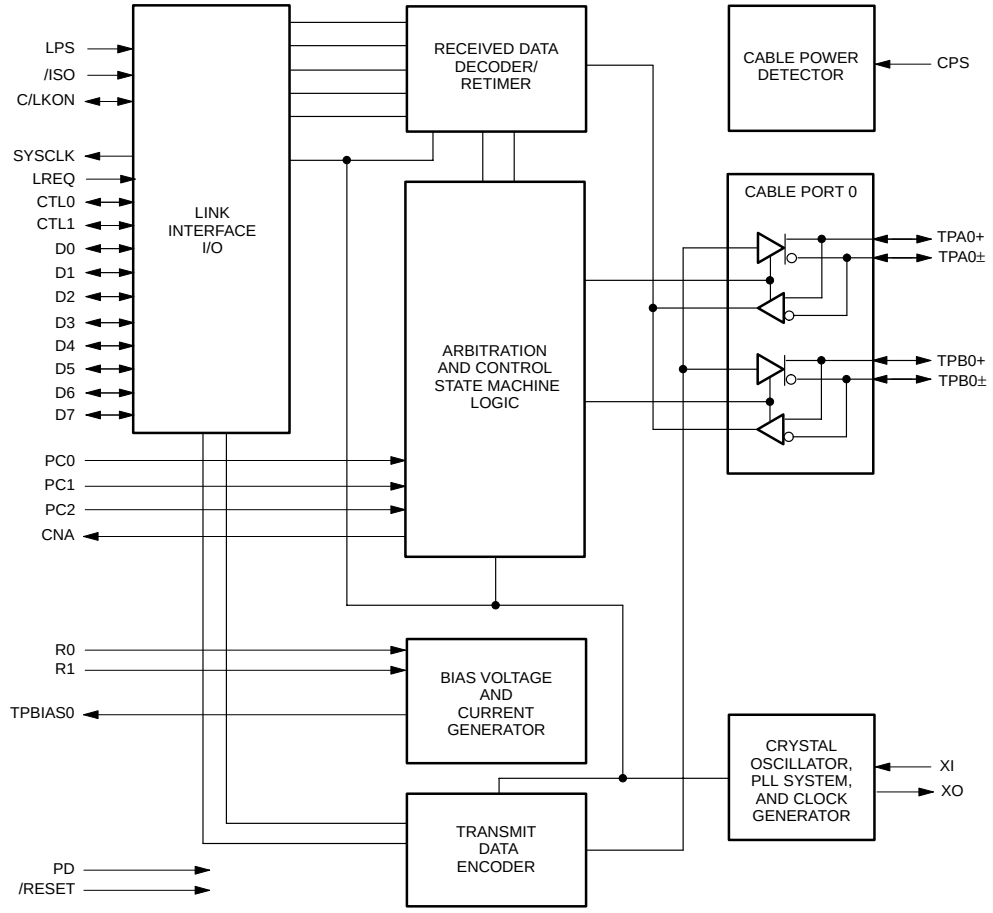
SAA7118: IC7500



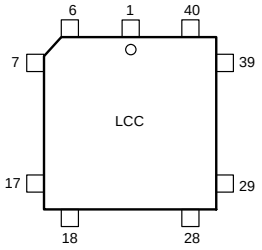


58PDI1394P25: IC7101



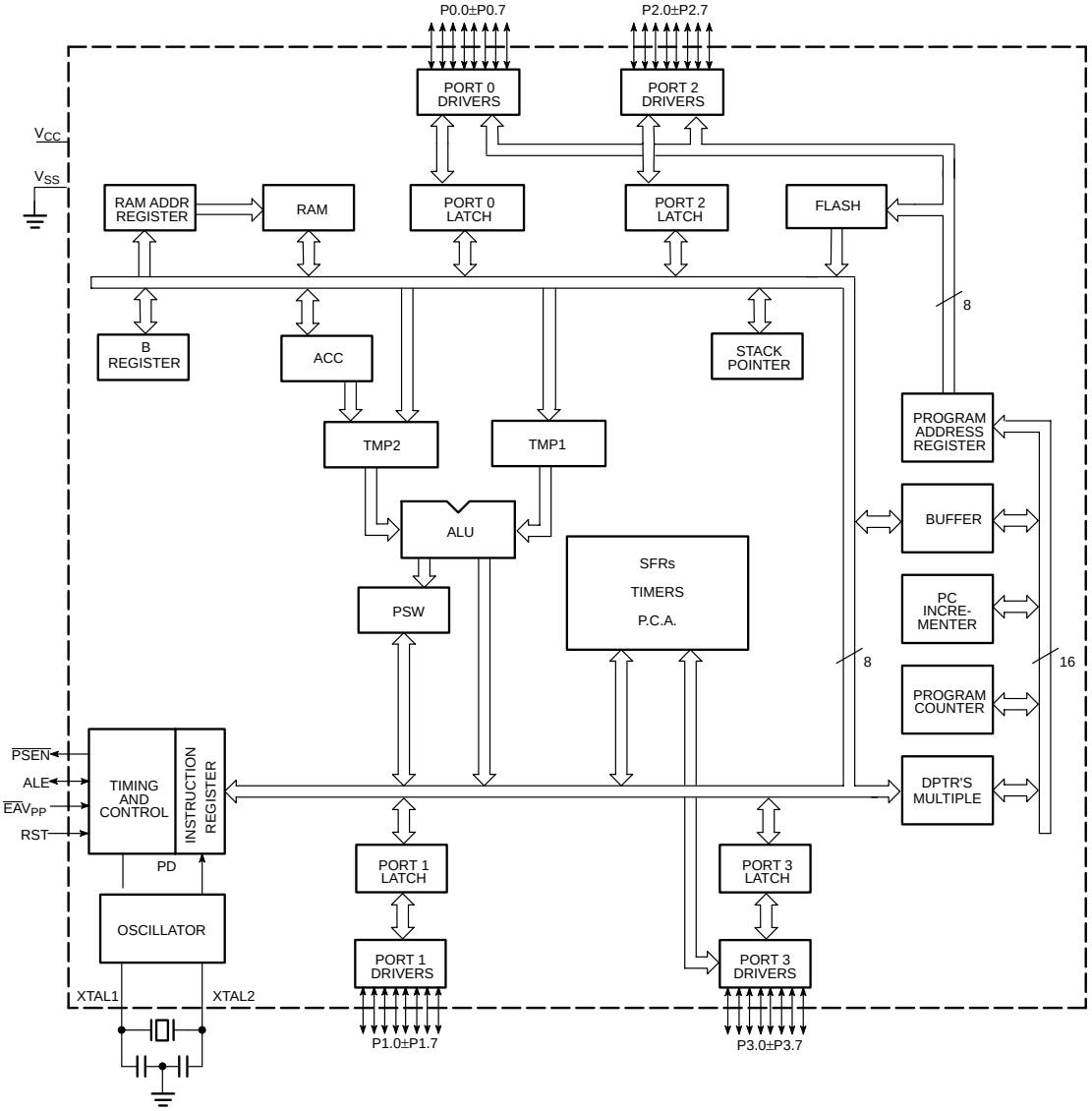


P89C51RD: IC7203

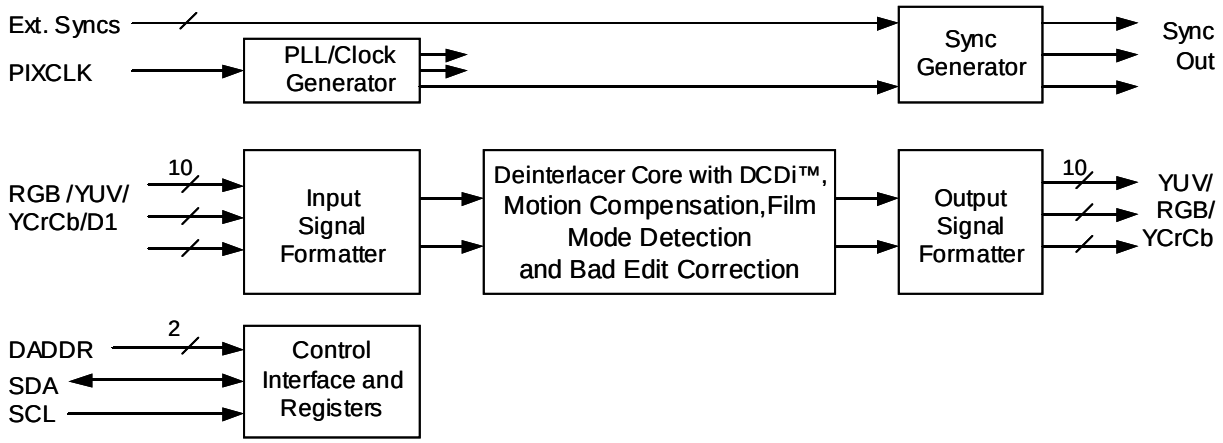


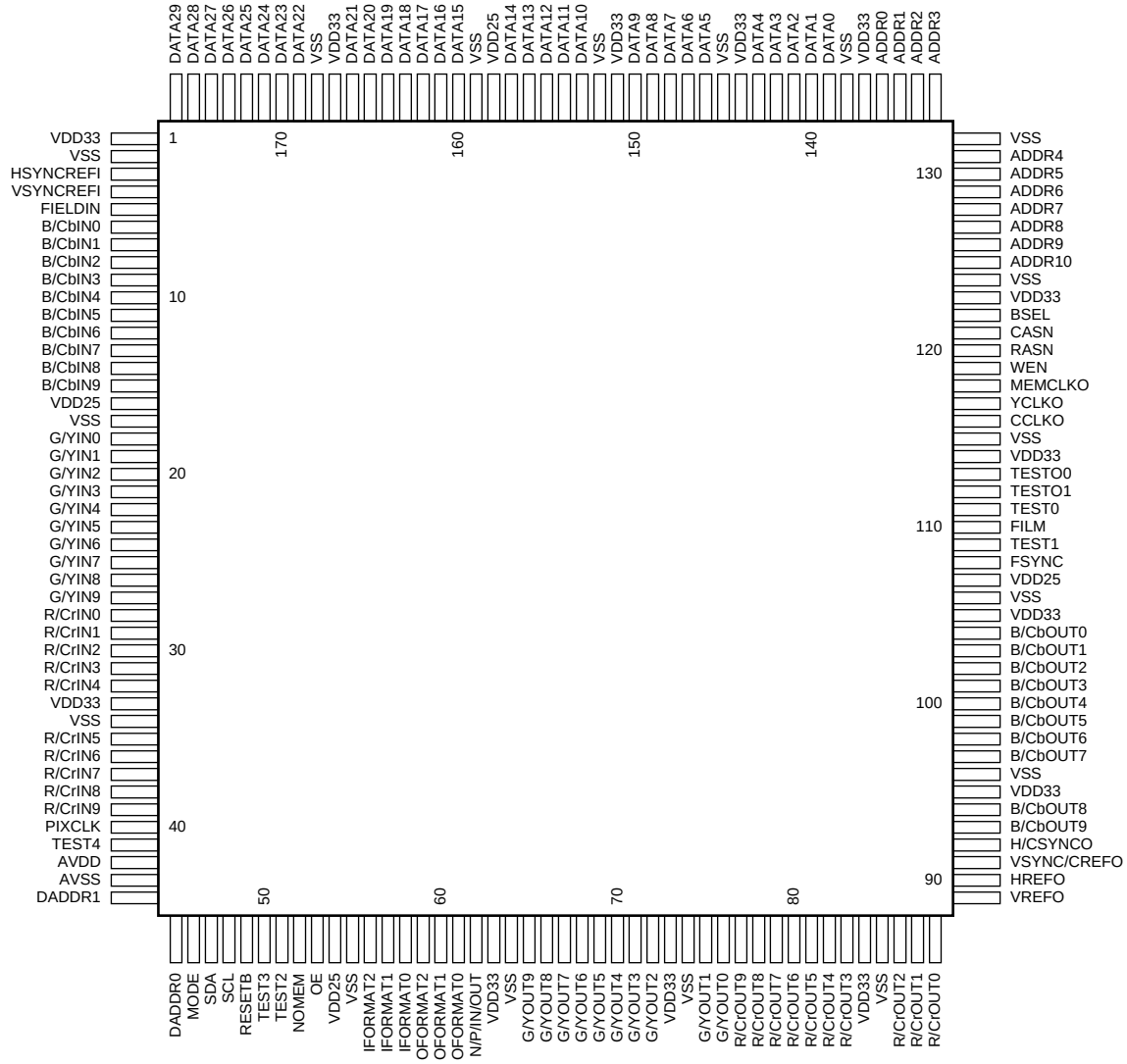
Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	$\overline{PSEN}$
3	P1.1/T2EX	18	P3.6/$\overline{WR}$	33	ALE/$\overline{PROG}$
4	P1.2/ECI	19	P3.7/$\overline{RD}$	34	NIC*
5	P1.3/CEX0	20	XTAL2	35	$\overline{EA}$/V_{PP}
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	V_{SS}	37	P0.6/AD6
8	P1.6/CEX3	23	NIC*	38	P0.5/AD5
9	P1.7/CEX4	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/$\overline{INT0}$	29	P2.5/A13	44	V_{CC}
15	P3.3/$\overline{INT1}$	30	P2.6/A14		

* NO INTERNAL CONNECTION



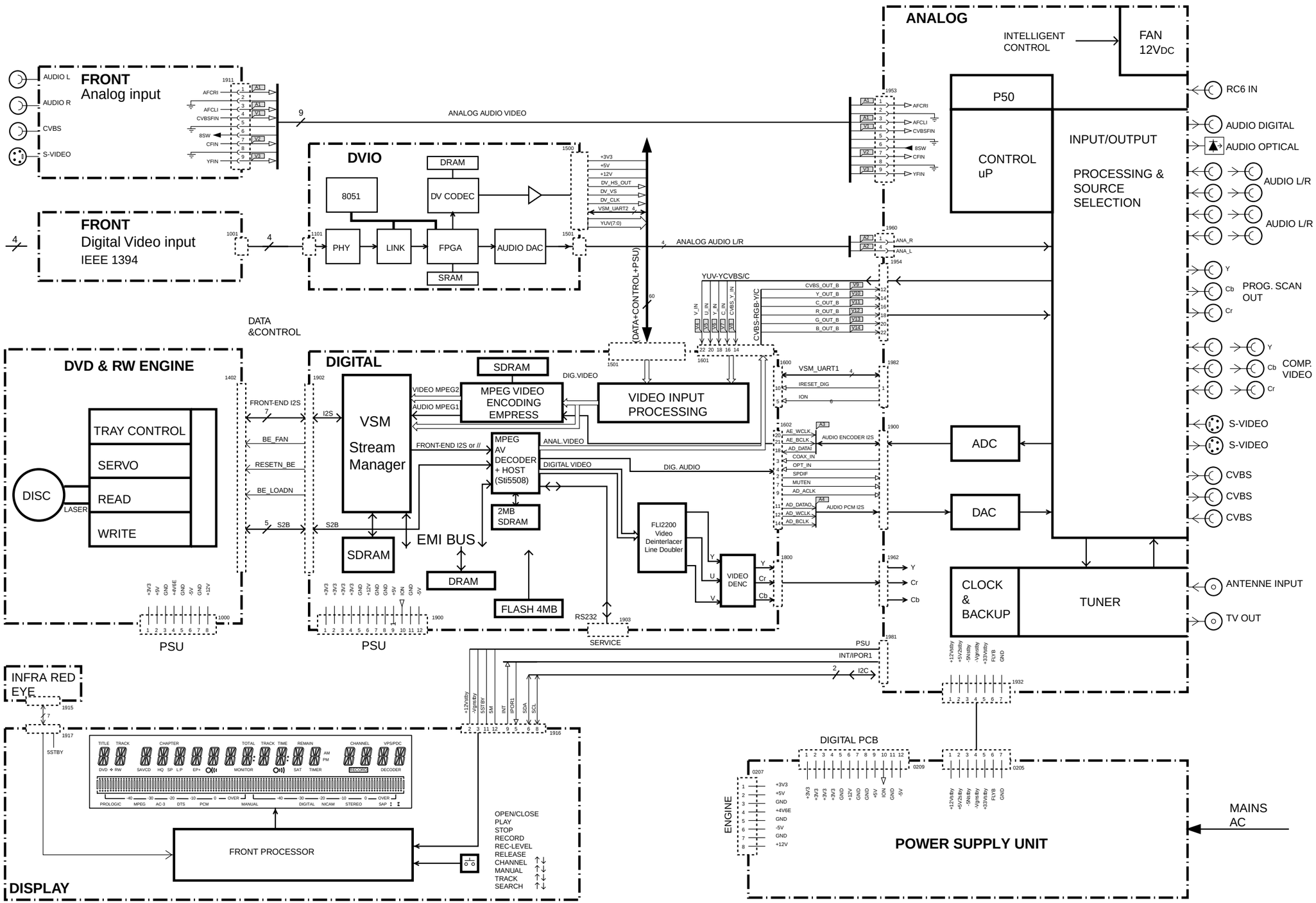
FLI2200


Ext. Syncs
PIXCLK
PLL/Clock Generator
Sync Generator
Sync Out
RGB /YUV/ YCrCb/D1
10
Input Signal Formatter
Deinterlacer Core with DCDi™, Motion Compensation,Film Mode Detection and Bad Edit Correction
Output Signal Formatter
10
YUV/ RGB/ YCrCb
DADDR
2
SDA
SCL
Control Interface and Registers

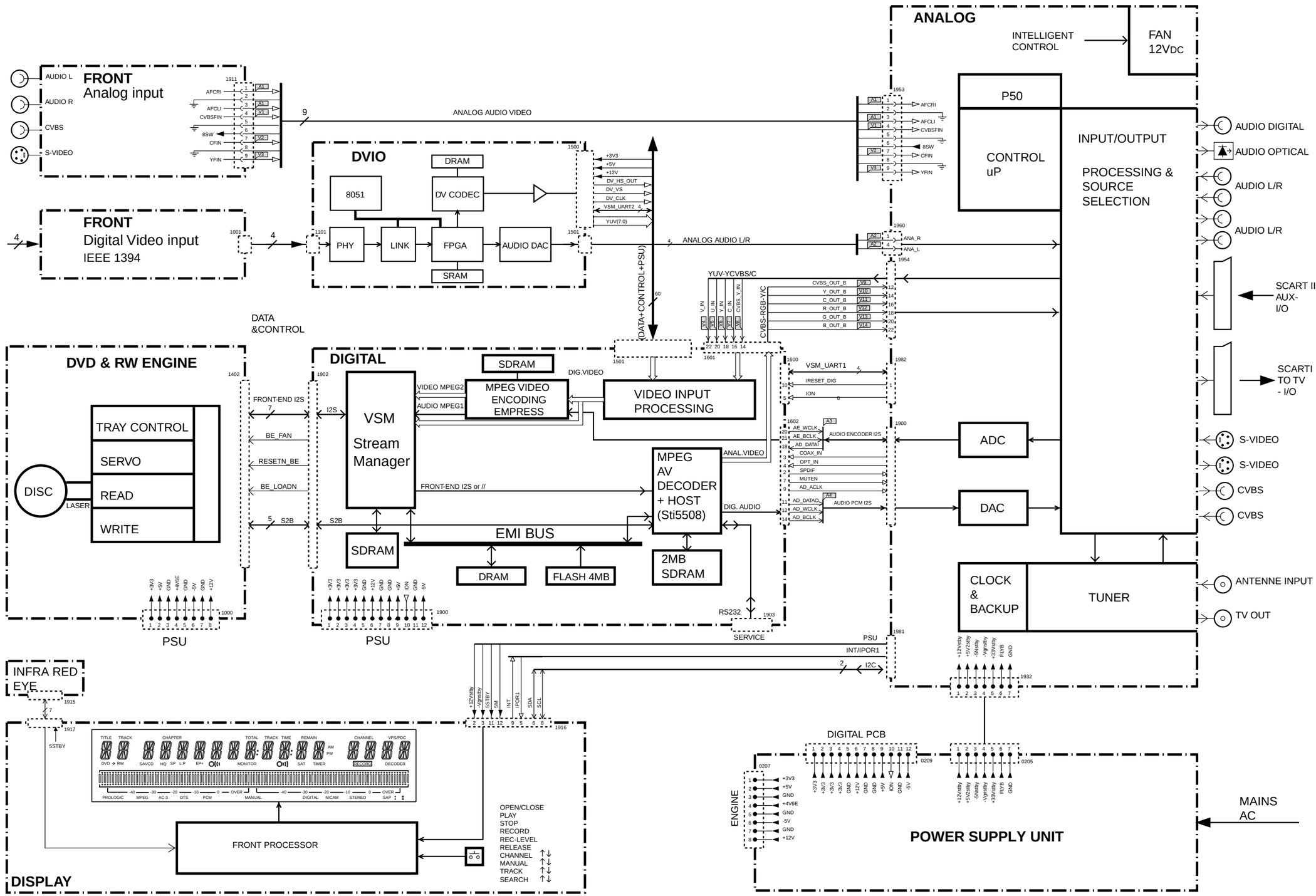

DATA29 DATA28 DATA27 DATA26 DATA25 DATA24 DATA23 DATA22 VSS VDD33 DATA21 DATA20 DATA19 DATA18 DATA17 DATA16 DATA15 VSS VDD25 DATA14 DATA13 DATA12 DATA11 DATA10 VSS VDD33 DATA9 DATA8 DATA7 DATA6 DATA5 VSS VDD33 DATA4 DATA3 DATA2 DATA1 DATA0 VSS VDD33 ADDR0 ADDR1 ADDR2 ADDR3
VDD33 VSS HSYNCREFI VSYNCREFI FIELDIN B/CbIN0 B/CbIN1 B/CbIN2 B/CbIN3 B/CbIN4 B/CbIN5 B/CbIN6 B/CbIN7 B/CbIN8 B/CbIN9 VDD25 VSS G/YIN0 G/YIN1 G/YIN2 G/YIN3 G/YIN4 G/YIN5 G/YIN6 G/YIN7 G/YIN8 G/YIN9 R/CrIN0 R/CrIN1 R/CrIN2 R/CrIN3 R/CrIN4 VDD33 VSS R/CrIN5 R/CrIN6 R/CrIN7 R/CrIN8 R/CrIN9 PIXCLK TEST4 AVDD AVSS DADDR1
1 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170
VSS ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 VSS VDD33 BSEL CASN RASN WEN MEMCLKO YCLKO CCLKO VSS VDD33 TESTO0 TESTO1 TEST0 FILM TEST1 FSYNC VDD25 VSS VDD33 B/CbOUT0 B/CbOUT1 B/CbOUT2 B/CbOUT3 B/CbOUT4 B/CbOUT5 B/CbOUT6 B/CbOUT7 VSS VDD33 B/CbOUT8 B/CbOUT9 H/CSYNCO VSYNC/CREFO HREFO VREFO
DADDR0 MODE SDA SCL RESETB TEST3 TEST2 NOMEM OE VDD25 VSS IFORMAT2 IFORMAT1 IFORMAT0 OFORMAT2 OFORMAT1 OFORMAT0 N/P/IN/OUT VDD33 VSS G/YOUT9 G/YOUT8 G/YOUT7 G/YOUT6 G/YOUT5 G/YOUT4 G/YOUT3 G/YOUT2 VDD33 VSS G/YOUT1 G/YOUT0 R/CrOUT9 R/CrOUT8 R/CrOUT7 R/CrOUT6 R/CrOUT5 R/CrOUT4 R/CrOUT3 VDD33 VSS R/CrOUT2 R/CrOUT1 R/CrOUT0

MEMO

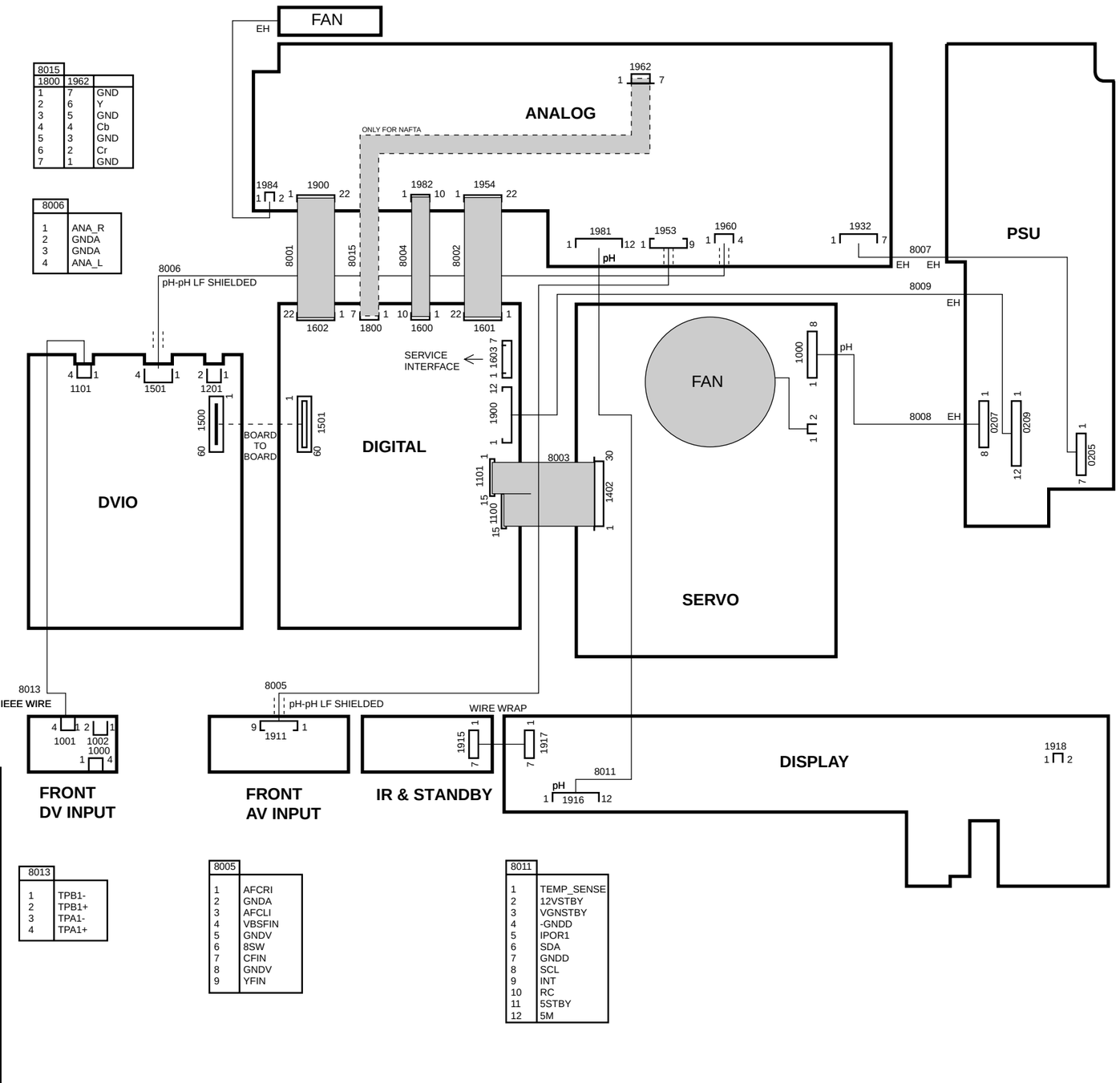
■ BLOCK DIAGRAM U model



■ BLOCK DIAGRAM **A, B, G model**



■ WIRING DIAGRAM



8001		
1602	1900	
1	22	GNDD
2	21	SPDIF
3	20	COAX_IN
4	19	OPT_IN
5	18	+5V
6	17	+3V3
7	16	MUTEN
8	15	GNDD
9	14	AD_ACLK
10	13	GNDD
11	12	AD_DATAO
12	11	AD_WCLK
13	10	GNDD
14	9	AD_BCLK
15	8	GNDD
16	7	AD_ACLK
17	6	GNDD
18	5	AD_DATAI
19	4	GNDD
20	3	AE_WCLK
21	2	AE_BCLK
22	1	GNDD

8002		
1601	1954	
1	22	B_OUT_B
2	21	GNDD
3	20	G_OUT_B
4	19	GNDD
5	18	R_OUT_B
6	17	GNDD
7	16	C_OUT_B
8	15	GNDD
9	14	Y_OUT_B
10	13	GNDD
11	12	CVBS_OUT_B
12	11	GNDD
13	10	GNDD
14	9	CVBS_Y_IN
15	8	GNDD
16	7	C_IN
17	6	GNDD
18	5	Y_IN
19	4	GNDD
20	3	U_IN
21	2	GNDD
22	1	V_IN

8003		
1100	1402	
15	1	GNDD
14	2	GNDD
13	3	NC
12	4	GNDD
11	5	BE_DATA_WR
10	6	GNDD
9	7	BE_SYNC
8	8	GNDD
7	9	BE_FLAG
6	10	GNDD
5	11	BE_BCLK
4	12	GNDD
3	13	BE_DATA_RD
2	14	GNDD
1	15	BE_WCLK
1101		
15	16	GNDD
14	17	BE_RXD
13	18	GNDD
12	19	BE_TXD
11	20	BE_CPR
10	21	BE_IRQn
9	22	BE_SUR
8	23	BE_V4
7	24	GNDD
6	25	BE_LOAD
5	26	GNDD
4	27	BE_FAN
3	28	RESETn_BE
2	29	GNDD
1	30	GNDD

8004		
1600	1982	
1	10	GNDD
2	9	FB
3	8	BE_FAN
4	7	ANA_WE
5	6	ION
6	5	VSM_UART1_RTSn (D_RDY)
7	4	VSM_UART1_CTSn (A_RDY)
8	3	VSM_UART1_TX (D_DATA)
9	2	VSM_UART1_RX (A_DATA)
10	1	IRESET_DIG

8015		
1800	1962	
1	7	GND
2	6	Y
3	5	GND
4	4	Cb
5	3	GND
6	2	Cr
7	1	GND

8006	
1	ANA_R
2	GNDA
3	GNDA
4	ANA_L

8014		
1200	1100	
1	24	GND
2	23	YUV_IN(7)
3	22	GND
4	21	YUV_IN(6)
5	20	+3V3
6	19	YUV_IN(5)
7	18	+3V3
8	17	YUV_IN(4)
9	16	+5V
10	15	YUV_IN(3)
11	14	GND
12	13	YUV_IN(2)
13	12	GND
14	11	YUV_IN(1)
15	10	GND
16	9	YUV_IN(0)
17	8	GND
18	7	CLK_27MHZ
19	6	GND
20	5	HS_IN
21	4	FRAME_IN
22	3	SCL
23	2	SDA
24	1	GND

8013	
1	TPB1-
2	TPB1+
3	TPA1-
4	TPA1+

8005	
1	AFCRI
2	GNDA
3	AFCLI
4	VBSFIN
5	GNDV
6	8SW
7	CFIN
8	GNDV
9	YFIN

8011	
1	TEMP_SENSE
2	12VSTBY
3	VGNSTBY
4	-GNDD
5	IPOR1
6	SDA
7	GNDD
8	SCL
9	INT
10	RC
11	5STBY
12	5M

8007	
1	+12Vstby
2	+5V2stby
3	-5Nstby
4	-Vgnstby
5	+33Vstby
6	FLYB
7	GND

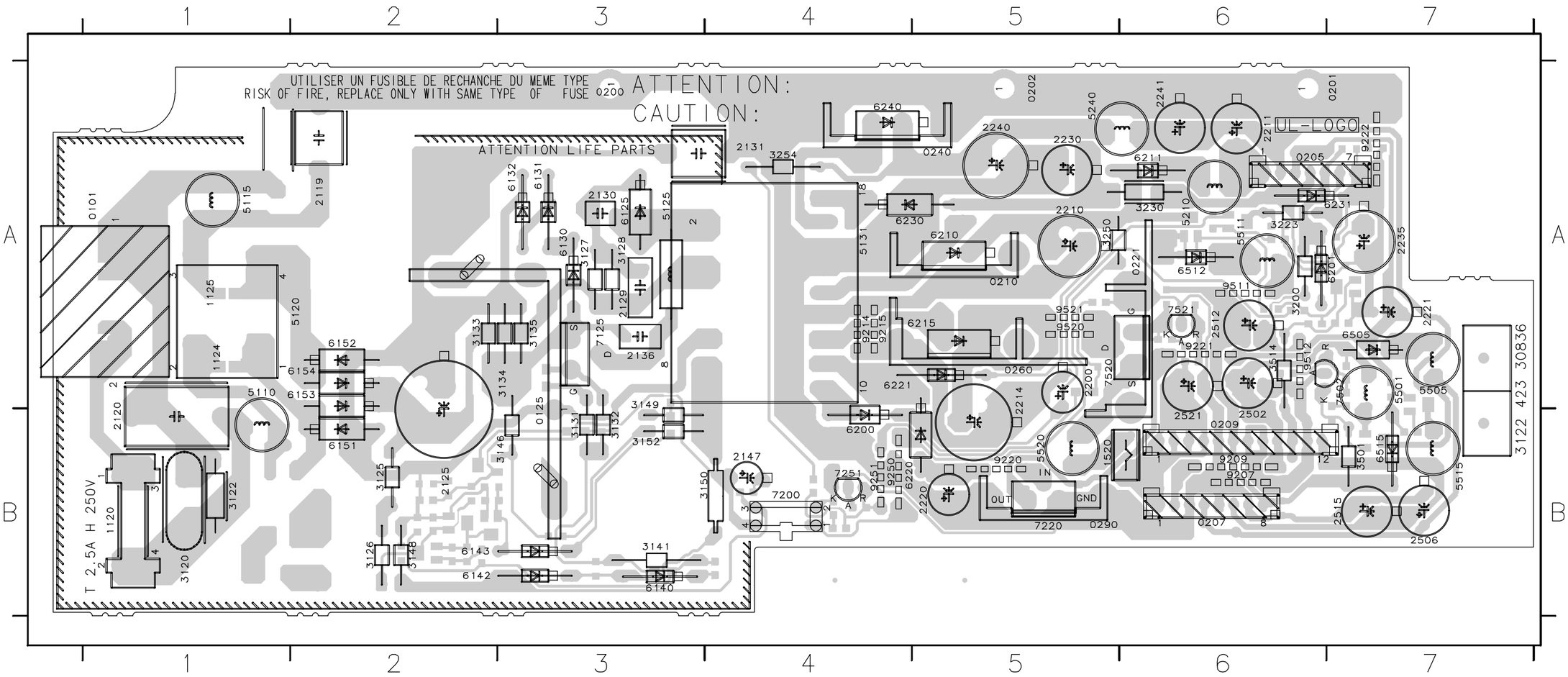
8008	
1	+3V3
2	+5V
3	GND
4	+4V6E
5	GND
6	-5V
7	GND
8	+12V

8009	
1	+3V3
2	+3V3
3	+3V3
4	+3V3
5	GNDD
6	+12V
7	GNDD
8	GNDD
9	+5V
10	ION(STBY_ctrl
11	GNDD
12	-5V

■ PRINTED CIRCUIT BOARD **A, B, G model**

POWER SUPPLY P. C. B. (Top View)

0101 A1	0209 B6	1520 B5	2130 A3	2212 A5	2240 A5	2521 B6	3128 A3	3141 B3	3223 A6	5115 A1	5501 A7	6129 B1	6151 B2	6211 A6	6505 A7	7502 A7	9214 A4	9511 A6
0125 B3	0210 A5	2119 A2	2131 A4	2214 A5	2241 A6	3120 B1	3129 B2	3146 B3	3230 A6	5120 A2	5505 A7	6130 A3	6152 A2	6215 A5	6512 A6	7520 A5	9215 A4	9512 A6
0200 A3	0221 A6	2120 B1	2136 A3	2215 A5	2242 A4	3122 B1	3131 B3	3148 B2	3250 A5	5121 A1	5511 A6	6131 A3	6153 A2	6220 B4	6515 B7	7521 A6	9220 B5	9512 A5
0201 A7	0240 A5	2125 B2	2147 B4	2220 B5	2502 B6	3123 A1	3132 B3	3149 A3	3254 A4	5125 A3	5515 B7	6132 A3	6154 A2	6221 A4	7125 A3	9110 B1	9221 A6	9521 A5
0202 A5	0260 A5	2126 B2	2200 A5	2221 A7	2506 B7	3125 B2	3133 A2	3150 B3	3501 B7	5131 A4	5520 B5	6140 B3	6200 B4	6230 A4	7200 B4	9115 A1	9222 A7	
0205 A6	0290 B5	2127 B1	2210 A5	2230 A5	2512 A6	3126 B2	3134 A3	3152 B3	3514 A6	5210 A6	6125 A3	6142 B2	6201 A7	6231 A7	7220 B5	9207 B6	9250 B4	
0207 B6	1120 B1	2129 A3	2211 A6	2235 A7	2515 B7	3127 A3	3135 A3	3200 A6	5110 A1	5240 A5	6128 B1	6143 B2	6210 A5	6240 A4	7251 B4	9209 B6	9251 B4	

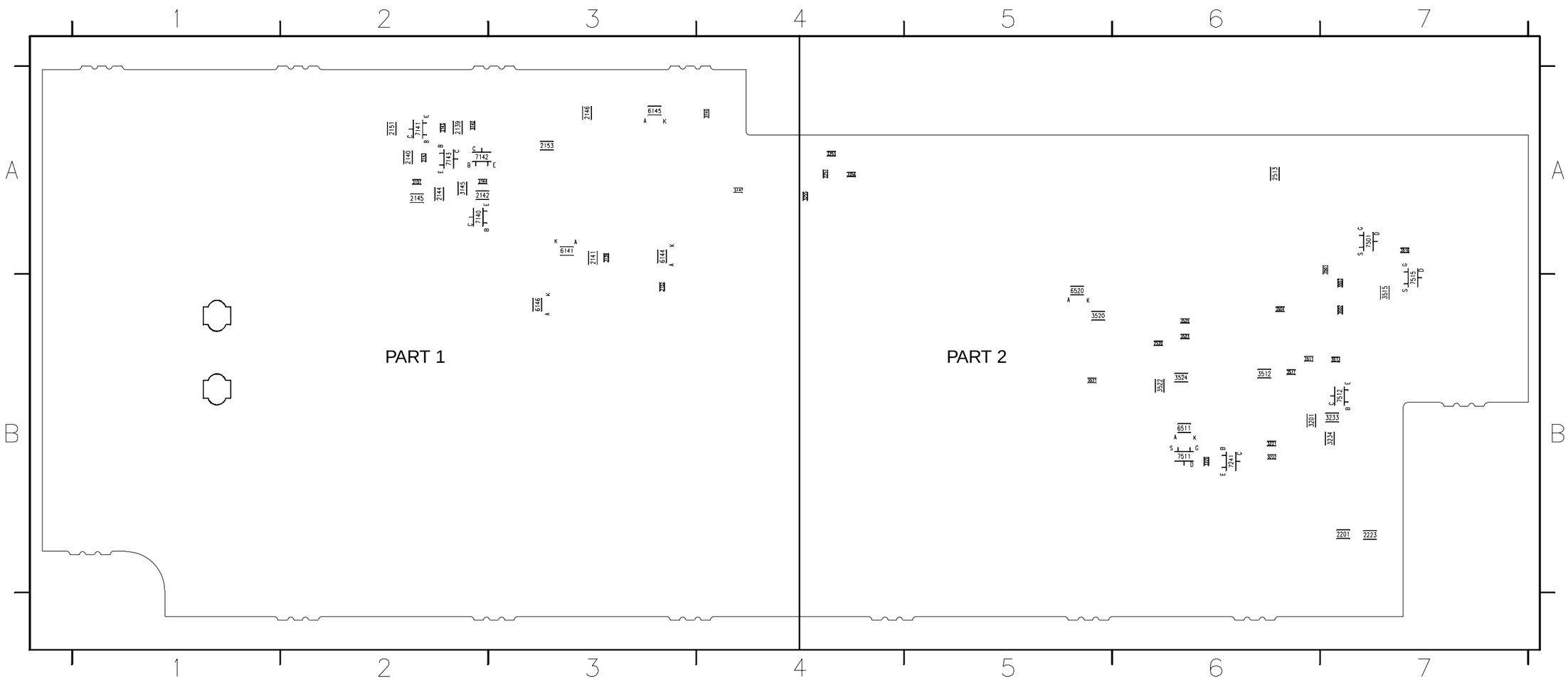


■ PRINTED CIRCUIT BOARD

A, B, G model

POWER SUPPLY P. C. B. (Bottom View)

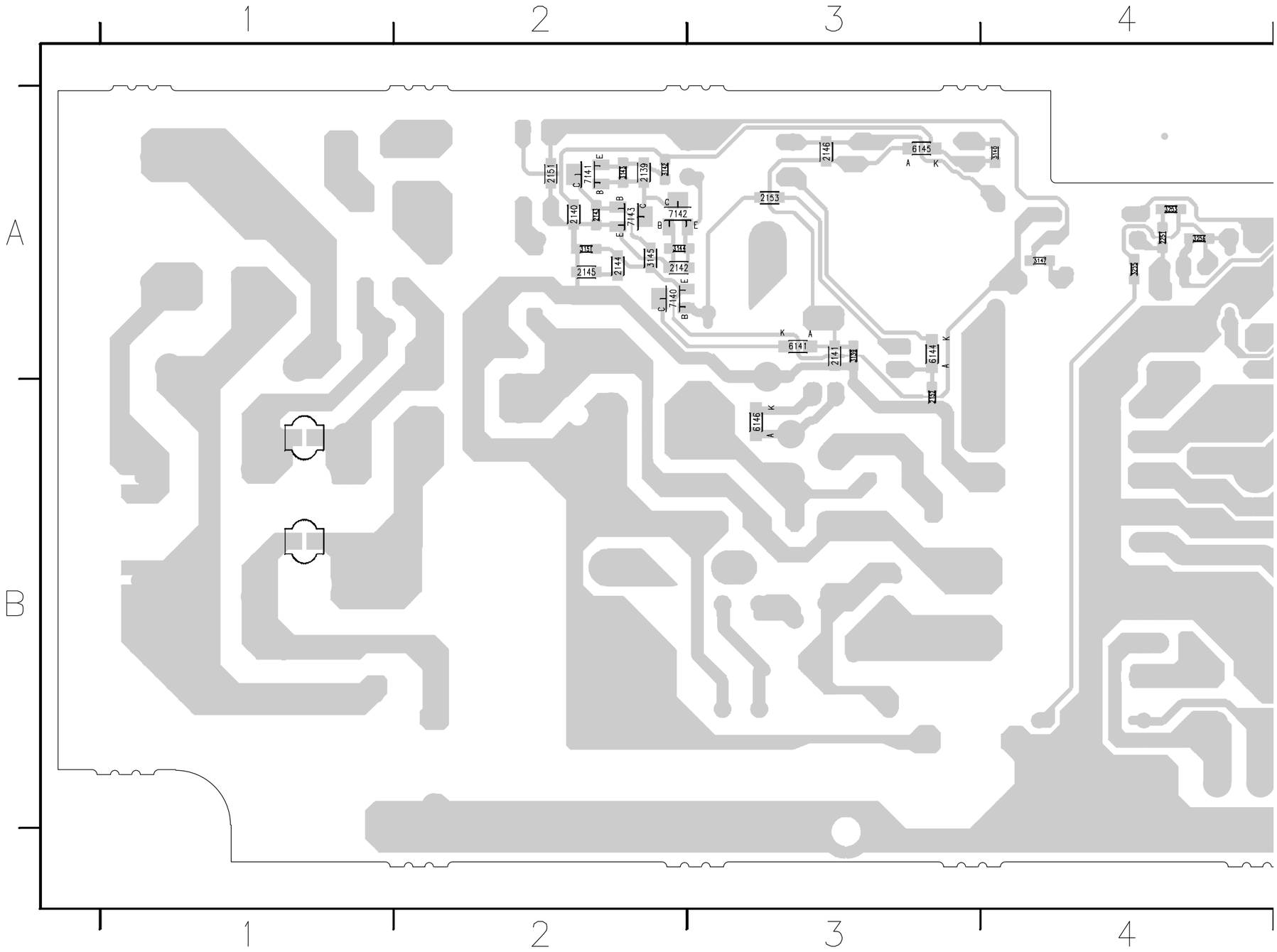
2139 A2	2143 A2	2151 A2	2222 A5	2511 B6	3140 A4	3145 A2	3220 B6	3234 B7	3502 B7	3512 B6	3520 B5	3524 B6	6145 A3	7140 A2	7241 B6	7515 B7	
2140 A2	2144 A2	2152 B3	2223 B7	2513 A6	3142 A2	3147 A4	3221 B6	3253 A4	3503 B7	3513 B7	3521 B5	3525 B6	6146 B3	7141 A2	7501 A7		
2141 A3	2145 A2	2153 A3	2251 A4	2520 B6	3143 A2	3151 A2	3222 B6	3255 A4	3504 B6	3515 B7	3522 B6	6141 A3	6511 B6	7142 A2	7511 B6		
2142 A2	2146 A3	2201 B7	2501 A7	3139 A3	3144 A2	3201 B6	3233 B7	3256 A4	3511 B6	3516 A7	3523 B6	6144 A3	6520 B5	7143 A2	7512 B7		



■ PRINTED CIRCUIT BOARD

A, B, G model

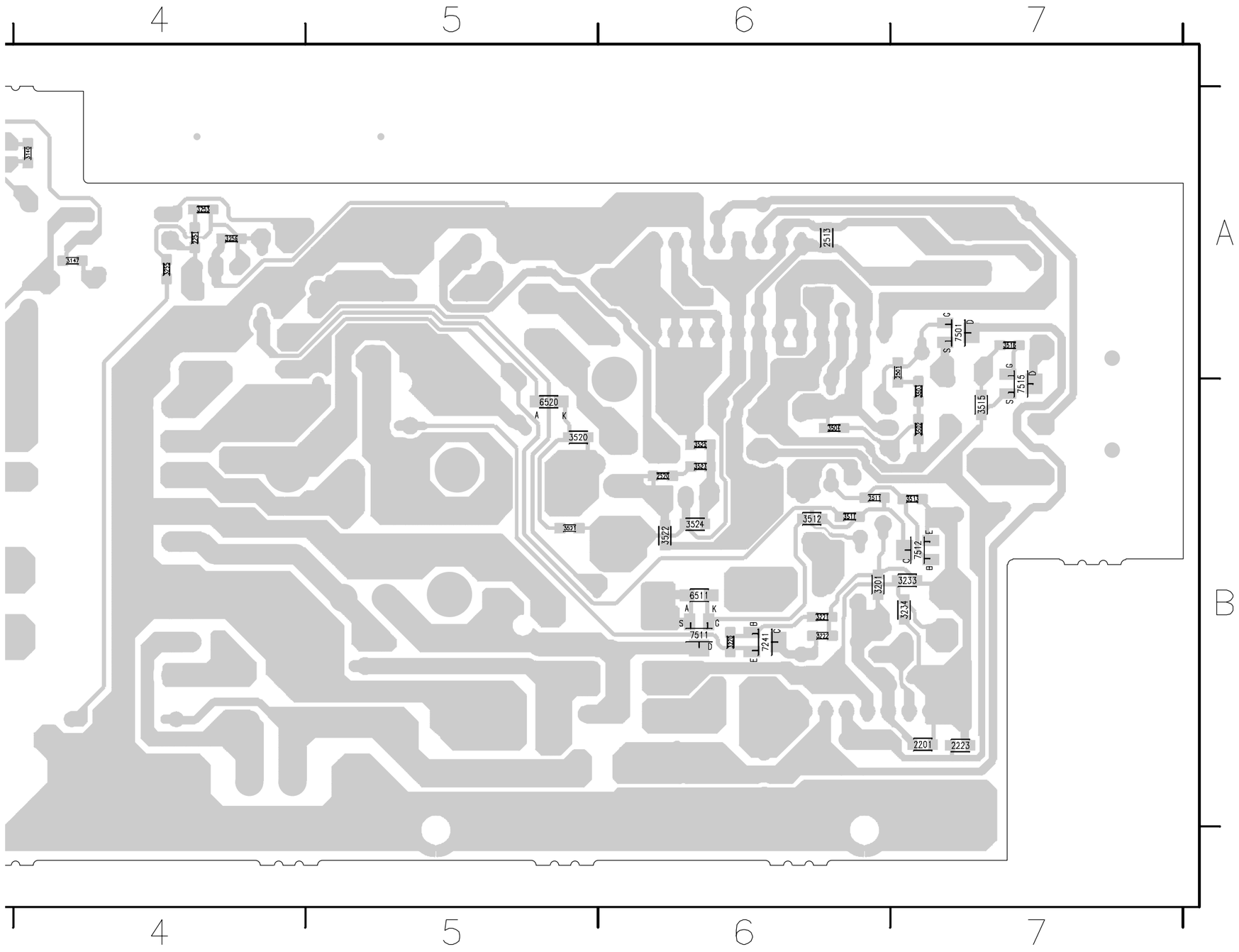
POWER SUPPLY P. C. B. **(Part 1 Top View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

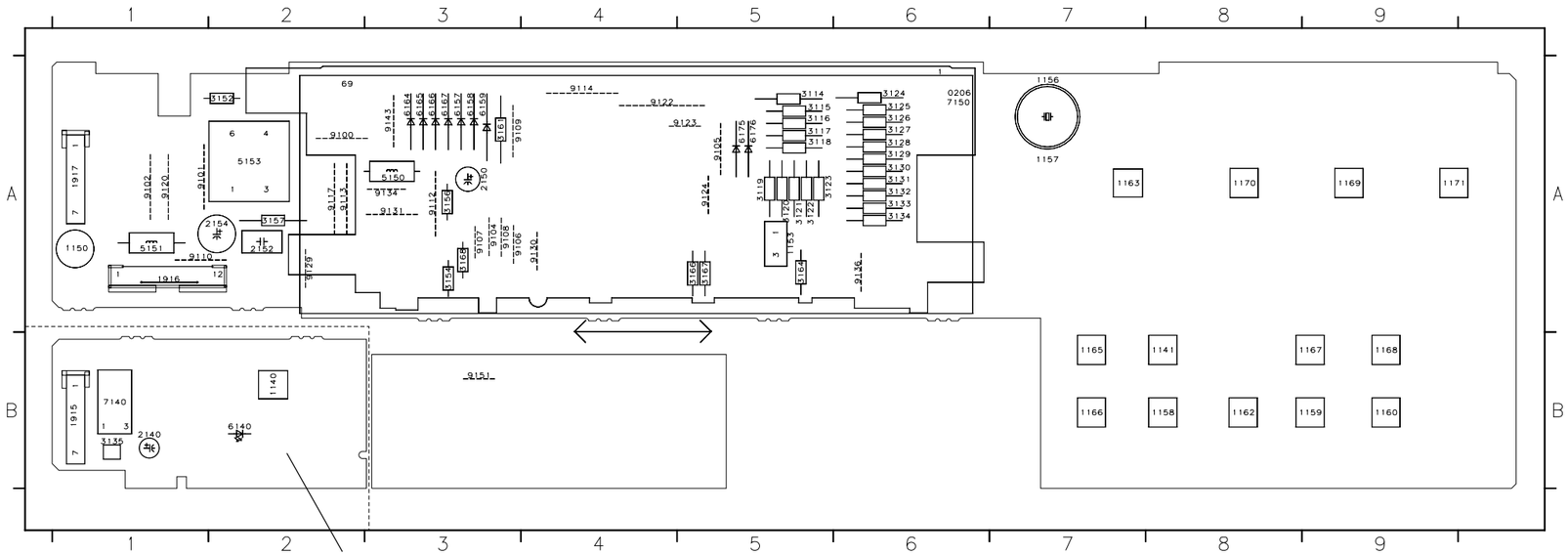
POWER SUPPLY P. C. B. **(Part 2 Top View)**



■ PRINTED CIRCUIT BOARD

DISPLAY P. C. B. (Top View)

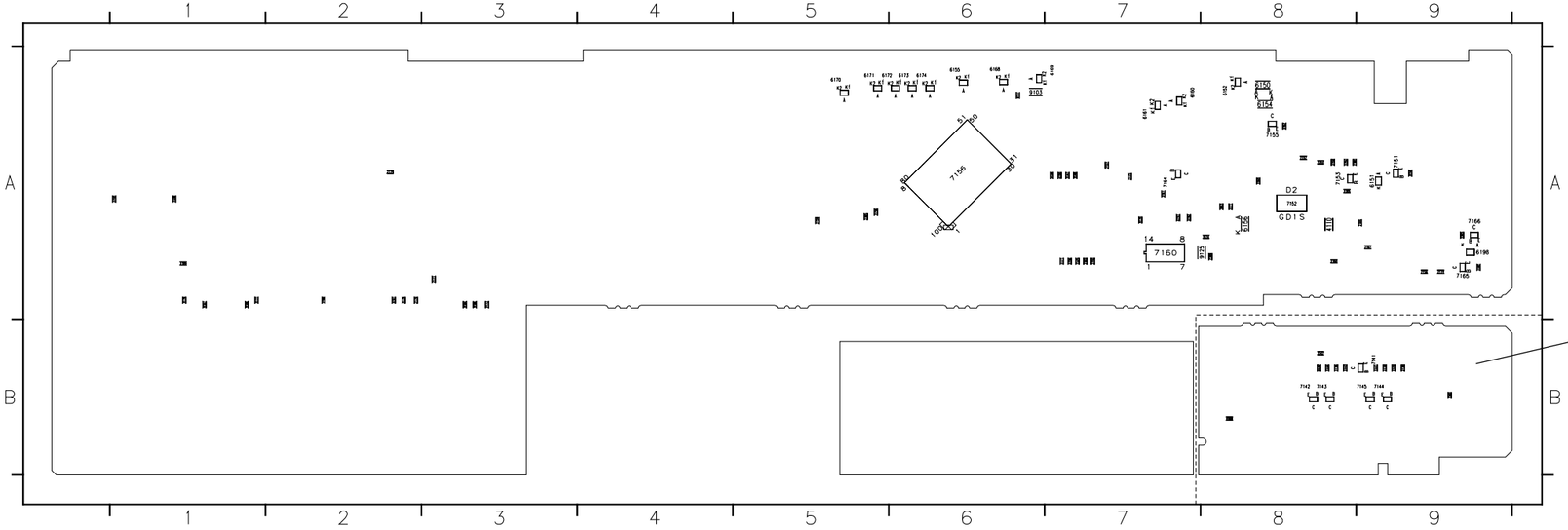
0206 A6 1140 B2 1141 B8 1150 A1 1153 A5 1156 A7 1157 A7 1158 B8 1159 B9 1160 B9 1161 A1 1162 B6 1163 A7 1165 B7 1166 B7 1167 B9 1168 B9 1169 A9 1170 A8 1171 A9 1910 B4 1911 B4 1916 A1 1917 A1 2140 B1 2150 A3 2152 A2 2153 A2 2154 A2 3110 B4 3114 A5 3116 A5 3117 A5 3118 A5 3119 A5 3120 A5 3121 A5 3122 A5 3123 A5 3124 A6 3125 A6 3126 A6 3127 A6 3128 A6 3129 A6 3130 A6 3131 A6 3132 A6 3133 A6 3134 B1 3152 A2 3154 A3 3156 A3 3157 A2 3161 A5 3164 A5 3166 A5 3167 A5 3168 A3 3179 A3 5150 A3 5151 A1 5153 A2 6140 B2 6157 A3 6158 A3 6159 A3 6164 A3 6165 A3 6166 A3 6167 A3 6175 A5 6176 A5 7140 B1 7150 A6 9100 A5 9101 A1 9102 A1 9104 A3 9105 A3 9106 A3 9107 A3 9108 A3 9109 A3 9110 A3 9112 A3 9113 A2 9114 A4 9117 A2 9120 A1 9122 A4 9123 A5 9124 A5 9129 A2 9130 A4 9131 A3 9136 A6 9143 A3 9151 B3



IR & STANDBY P. C. B. (Top View)

DISPLAY P. C. B. (Bottom View)

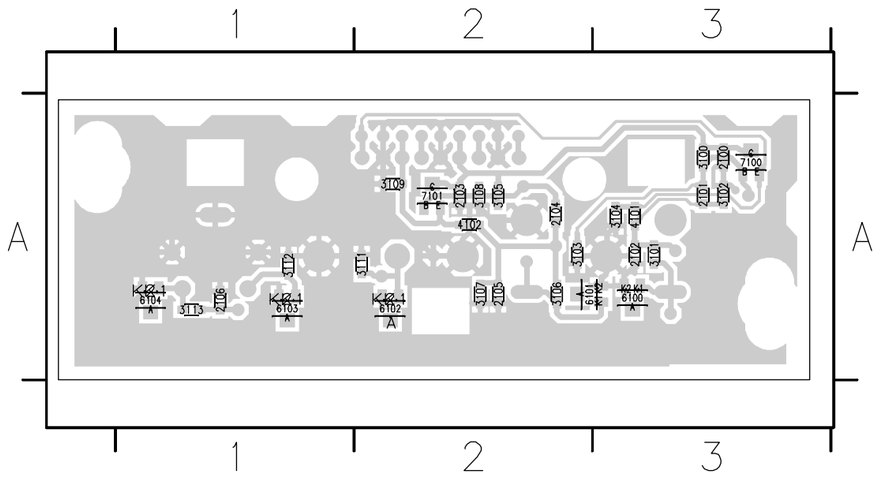
2100 B7 2101 B7 2102 B7 2103 B7 2104 B7 2105 B7 2106 B5 2151 A7 2155 A9 2156 A9 2157 A8 2158 A5 2159 A5 2160 A8 2161 A9 2162 A5 2163 A5 2167 A7 2168 A8 2169 A8 2170 A9 2171 A8 2173 A3 2174 A9 2175 A7 2177 A3 2179 A2 2180 A8 3100 B7 3101 B7 3102 B7 3103 B7 3104 B7 3105 B7 3106 B7 3107 B7 3108 B7 3109 B7 3111 B6 3112 B6 3113 B5 3136 B8 3137 B8 3138 B9 3139 B9 3140 B9 3141 B9 3142 B8 3143 B8 3144 B8 3145 A9 3146 A7 3147 A7 3148 A7 3149 B9 3150 A8 3151 A7 3152 A8 3155 A8 3158 A8 3159 A9 3160 A8 3162 A8 3163 A8 3165 A9 3169 A8 3170 A7 3171 A7 3172 A8 3173 A8 3174 A8 3176 A2 3177 A1 3178 A1 3180 A2 3182 A9 3183 A7 3184 A3 3185 A3 3186 A1 3187 A1 3188 A1 3189 A1 3190 A1 3191 A2 3192 A7 3193 A7 3194 A7 4100 A7 4101 B7 4102 B7 4110 A8 4151 A9 4990 B8 6100 B7 6101 B7 6102 B6 6103 B6 6104 B6 6120 A8 6151 A9 6152 A8 6154 A8 6155 A6 6156 A8 6160 A7 6161 A7 6168 A6 6169 A7 6170 A6 6171 A5 6172 A5 6173 A6 6174 A6 6198 A9 7100 B7 7101 B7 7140 B1 7141 B9 7142 B8 7143 B8 7144 B9 7145 B9 7150 A6 7151 A9 7152 A8 7153 A8 7154 A8 7155 A9 7156 A6 7157 A8 7160 A7 7164 A7 7165 A9 7166 A9 9103 A6 9125 A8 9127 A6



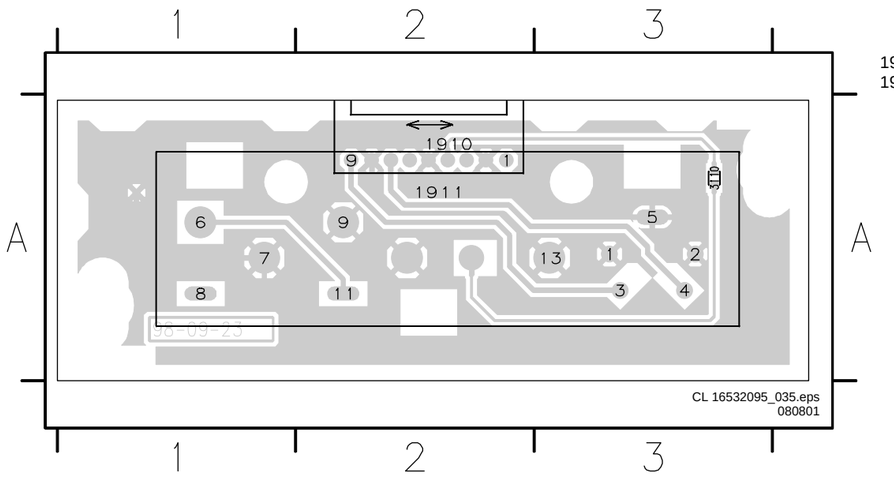
IR & STANDBY P. C. B. (Bottom View)

■ PRINTED CIRCUIT BOARD

FRONT AV INPUT P. C. B.

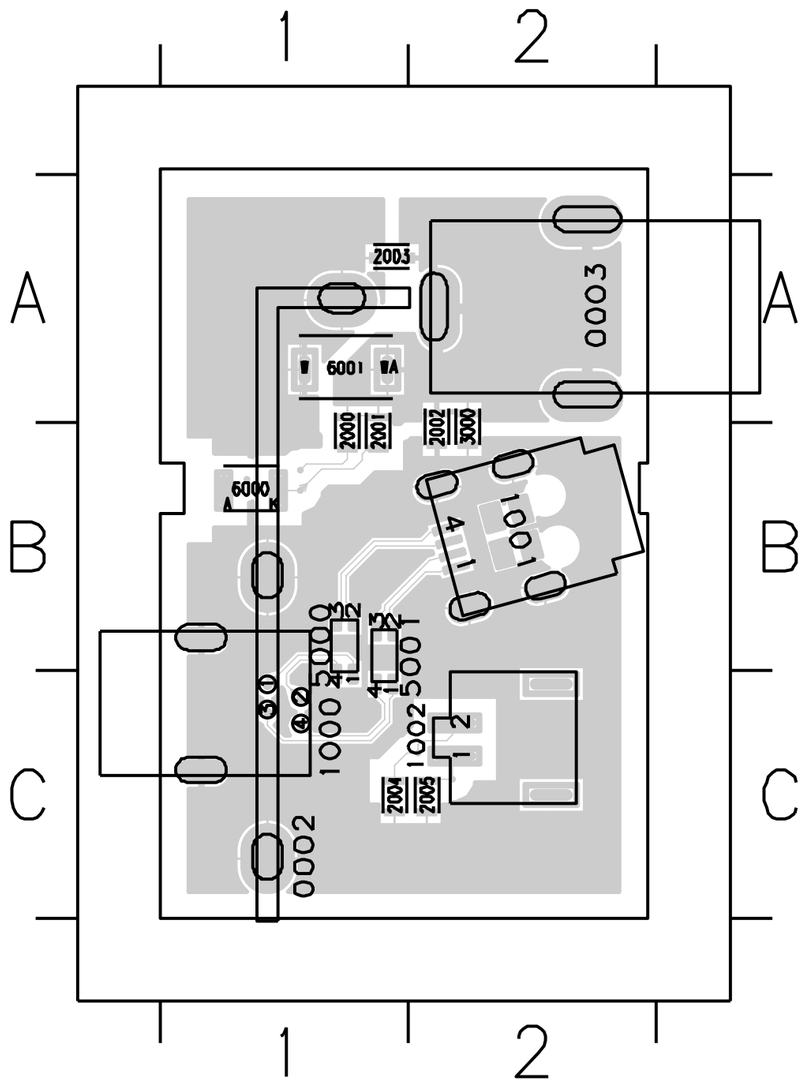


2100	A3	3113	A1
2101	A3	4101	A3
2102	A3	4102	A2
2103	A2	6100	A3
2104	A2	6101	A3
2105	A2	6102	A2
2106	A1	6103	A1
3100	A3	6104	A1
3101	A3	7100	A3
3102	A3	7101	A2
3103	A3		
3104	A3		
3105	A2		
3106	A2		
3107	A2		
3108	A2		
3109	A2		
3111	A1		
3112	A1		



1910	A2		
1911	A2		

FRONT DV INPUT P. C. B.

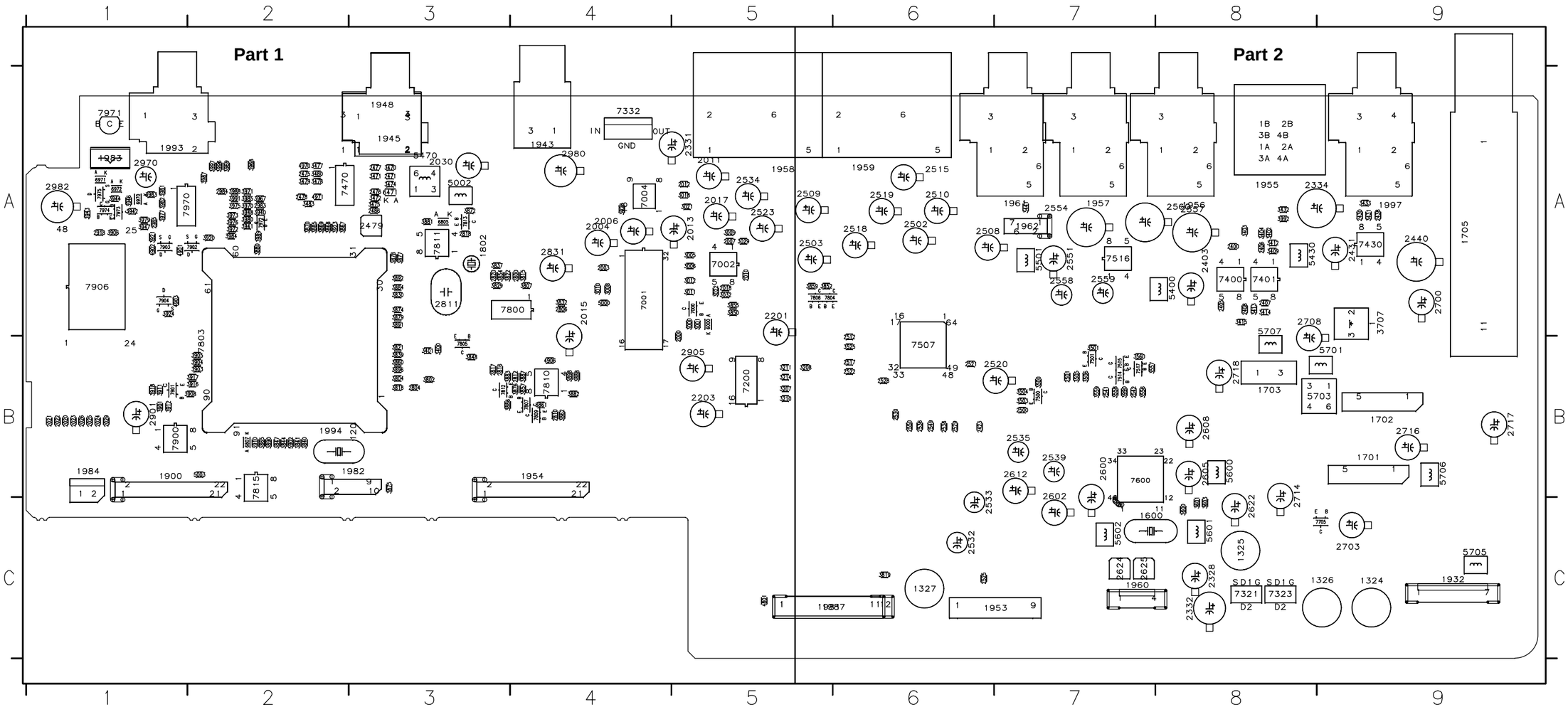


0002	C1		
0003	A2		
1000	C1		
1001	B2		
1002	C2		
2000	B1		
2001	B1		
2002	B2		
2003	A1		
2004	C1		
2005	C2		
3000	B2		
5000	B2		
5001	B2		
6000	B1		
6001	A1		

■ PRINTED CIRCUIT BOARD **U model**

ANALOG P. C. B. (Overview Top View)

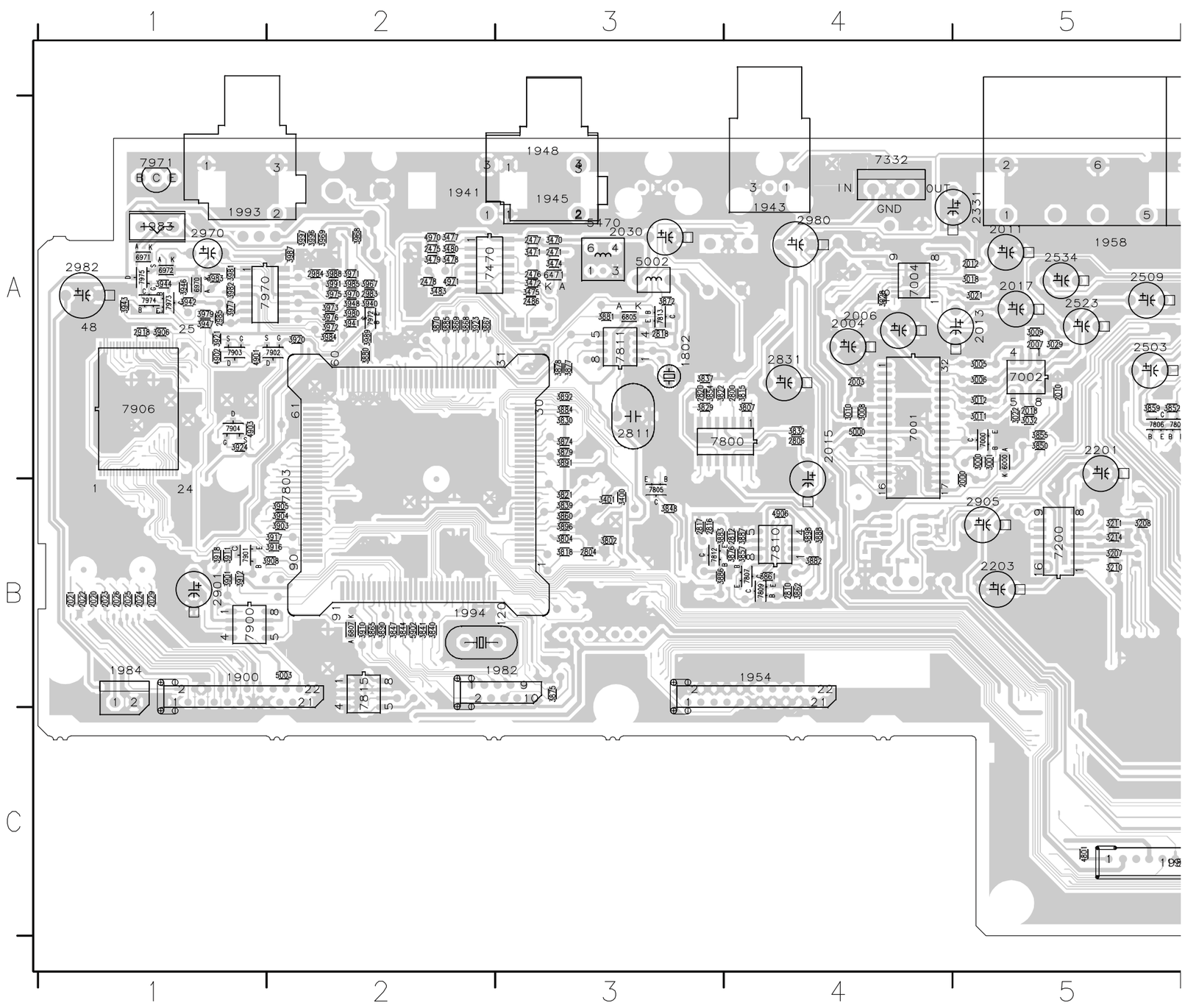
1324	C9	1953	C7	2000	B5	2030	A3	2475	A2	2523	A5	2558	A7	2810	B4	3006	A5	3403	A8	3500	B7	3819	C6	3862	B4	3888	B4	3924	A1	3981	A1	4971	A2	6805	A3	7507	B6	7901	B1
1325	C8	1954	B4	2003	A4	2201	A5	2476	A3	2525	C6	2559	A7	2811	A3	3008	A4	3404	A8	3501	B7	3821	B3	3865	B2	3890	B2	3940	A2	3982	A1	5000	A4	6807	B2	7513	B4	7902	A2
1326	C9	1955	A8	2004	A4	2203	B5	2477	A3	2528	B6	2560	A8	2812	B4	3009	A5	3409	A8	3503	B7	3822	A3	3867	A2	3891	A3	3941	A2	3983	A1	5002	A3	6970	A1	7514	B7	7903	A1
1327	C6	1956	A8	2006	A4	2328	C8	2478	A2	2529	B6	2600	B7	2813	A3	3010	A4	3412	A8	3504	B7	3829	A3	3868	A2	3892	A3	3942	A1	3984	A2	5003	B2	6971	A1	7515	B7	7904	A1
1600	C7	1957	A7	2007	A5	2330	A4	2479	A3	2530	B6	2602	B7	2816	B3	3011	A5	3413	A8	3505	B7	3830	A3	3869	A2	3896	B3	3943	A1	3985	A2	5400	A8	6972	A1	7516	A7	7906	A1
1700	C9	1958	A5	2010	A5	2331	A5	2486	A3	2532	C6	2605	B8	2817	B3	3012	A5	3414	A8	3506	B7	3832	A4	3870	A2	3898	B4	3944	A1	3987	A2	5430	A8	7000	A5	7517	B7	7970	A1
1701	B9	1959	A6	2011	A5	2332	C8	2500	B7	2533	C6	2608	B8	2818	A3	3018	A5	3415	A8	3525	B6	3837	A3	3872	A3	3901	B1	3946	A1	3988	A2	5470	A3	7001	A4	7600	B7	7971	A1
1702	B9	1960	C7	2012	A5	2334	A8	2501	B7	2534	A5	2612	B7	2820	A3	3021	A5	3431	A9	3556	B7	3839	B3	3874	A3	3903	B2	3947	A1	3989	A2	5501	A7	7002	A5	7705	C9	7972	A2
1703	B8	1961	A7	2013	A5	2400	A8	2502	A6	2535	B7	2622	C8	2831	A4	3022	A5	3432	A8	3557	B7	3840	B2	3875	B3	3904	B2	3948	A2	3990	B7	5600	B8	7004	A4	7800	A4	7973	A1
1705	A9	1962	A7	2015	A4	2403	A8	2503	A5	2536	B6	2624	C7	2901	B1	3028	A4	3433	A9	3558	B7	3841	B2	3876	B4	3905	B2	3967	A2	3991	A2	5601	C8	7005	A4	7803	B2	7974	A1
1802	A3	1980	B3	2017	A5	2405	A8	2508	A6	2538	B6	2625	C7	2905	B5	3029	A5	3441	A7	3559	B7	3844	B2	3877	A3	3906	A1	3968	A2	3992	A8	5602	C7	7200	B5	7804	A5	7975	A1
1900	B1	1981	C5	2018	A5	2406	A8	2509	A5	2539	B7	2700	A9	2918	A1	3032	A5	3470	A3	3560	B7	3847	B2	3878	A3	3908	B2	3969	A2	3996	A2	5701	B9	7321	C8	7805	B3		
1910	C3	1982	B3	2020	B1	2407	A8	2510	A6	2541	B7	2703	C9	2970	A1	3110	C4	3471	A3	3600	C8	3848	B3	3879	A3	3910	B2	3970	A2	3997	A2	5702	C9	7323	C8	7806	A5		
1911	C3	1983	A1	2021	B1	2408	A8	2512	B6	2542	B7	2708	A8	2980	A4	3207	B5	3472	A3	3601	C8	3850	A5	3880	A2	3911	B1	3971	A2	4405	B4	5703	B9	7332	A4	7807	B4		
1932	C9	1984	B1	2022	B1	2423	B6	2515	A6	2549	B6	2714	B8	2982	A1	3208	B5	3474	A3	3603	C8	3852	A5	3881	A3	3912	B1	3972	A2	4406	B4	5704	B9	7400	A8	7809	B4		
1941	A2	1987	C6	2023	B1	2430	A9	2517	B6	2550	B6	2716	B9	2983	A2	3210	B5	3475	A3	3707	A9	3854	A3	3882	B4	3916	B2	3973	A2	4801	C5	5705	C9	7401	A8	7810	B4		
1942	A3	1992	A2	2024	B1	2431	A9	2518	A6	2551	A7	2717	B9	2984	A2	3211	B5	3477	A2	3802	B3	3855	A5	3883	B3	3917	B2	3975	A2	4901	A1	5706	B9	7430	A9	7811	A3		
1943	A4	1993	A1	2025	B1	2438	A9	2519	A6	2553	B4	2718	B8	2985	A1	3214	B5	3478	A2	3804	B3	3857	B4	3884	A3	3918	B1	3976	A2	4902	A1	5707	A8	7432	A2	7812	B3		
1945	A3	1994	B2	2026	B1	2440	A9	2520	B7	2554	A7	2800	A4	3000	A5	3400	B3	3479	A2	3807	A4	3859	A5	3885	A2	3920	A2	3977	A1	4903	A1	5902	B2	7470	A2	7813	A3		
1948	A3	1996	C9	2028	A4	2444	A2	2521	B6	2555	B4	2804	B3	3001	A5	3401	B3	3480	A2	3815	A4	3860	B3	3886	B3	3921	A1	3979	A1	4906	B4	6000	A5	7500	B7	7815	B2		
1951	B4	1997	A9	2029	B1	2471	A3	2522	B6	2557	A8	2806	A4	3005	A5	3402	A8	3483	A2	3818	B3	3861	B4	3887	B4	3923	A2	3980	A2	4970	A2	6471	A3	7501	B7	7900	B1		



■ PRINTED CIRCUIT BOARD

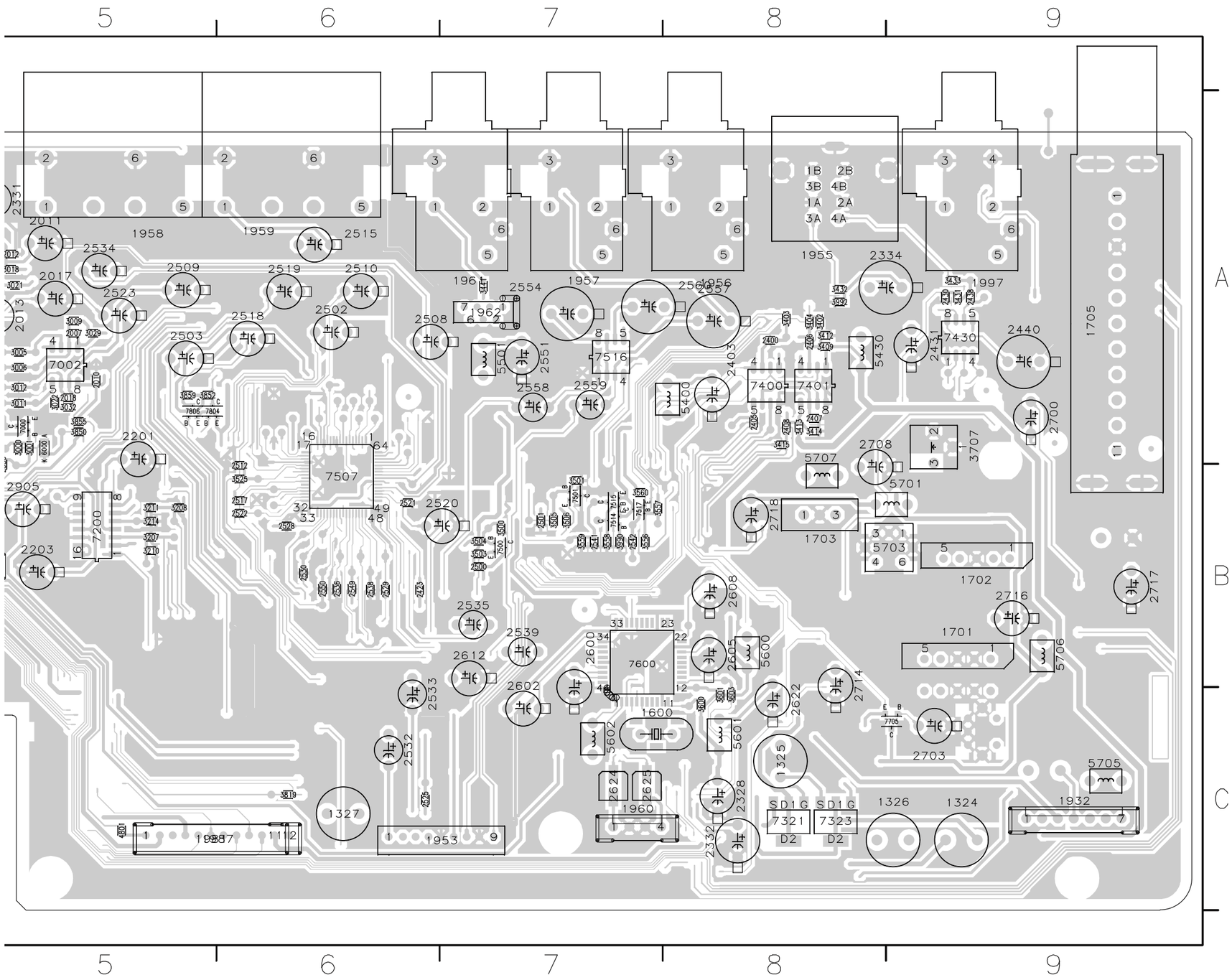
U model

ANALOG P. C. B. **(Part 1 Top View)**



■ PRINTED CIRCUIT BOARD **U model**

ANALOG P. C. B. **(Part 2 Top View)**



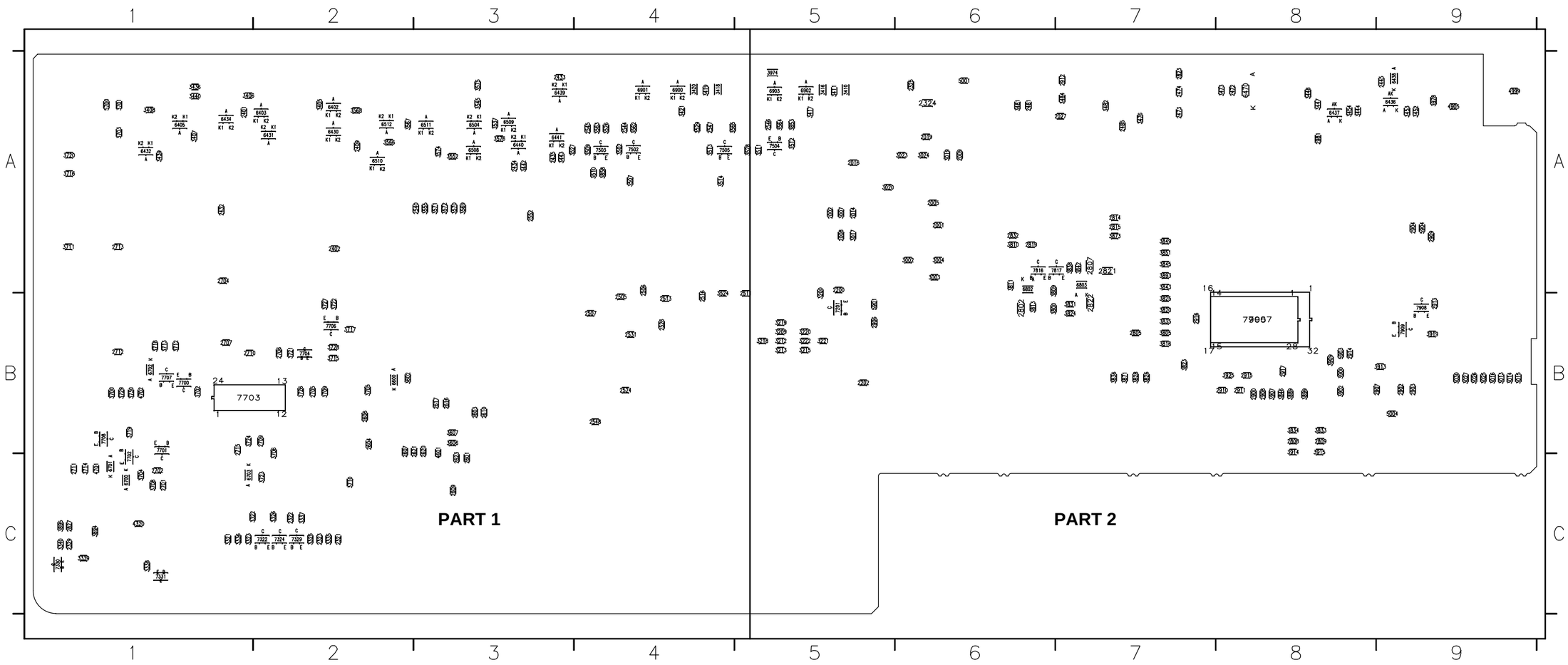
■ PRINTED CIRCUIT BOARD

U model

ANALOG P. C. B. (Overview Bottom View)

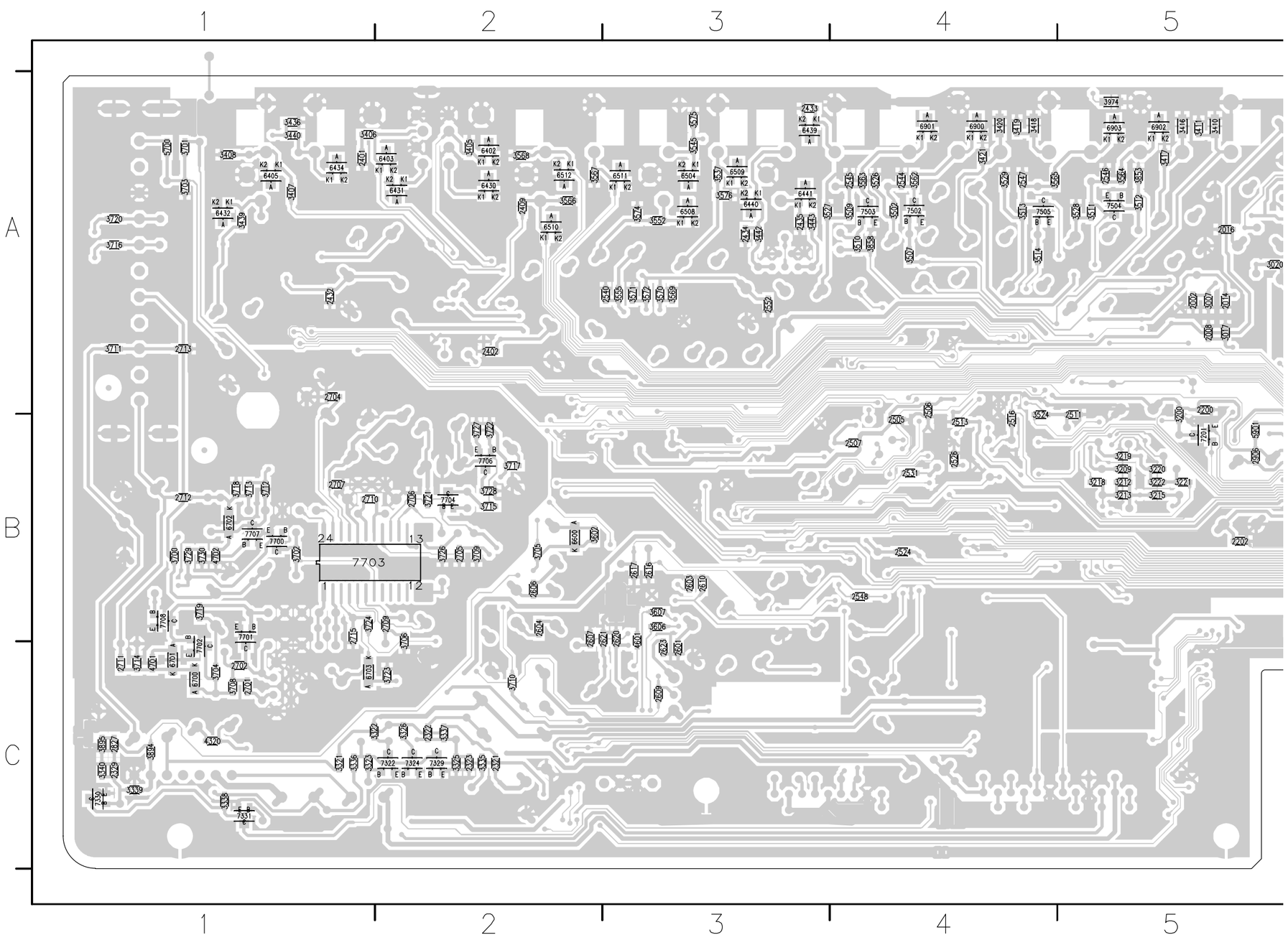
2001	A6	2321	C2	2472	A8	2607	B2	2715	B1	2907	B9	3016	B9	3109	C6	3329	A4	3416	A5	3481	A6	3564	A5
2002	A3	2322	C2	2473	A7	2609	C3	2802	B6	2908	B8	3017	A5	3111	C6	3335	C2	3417	A5	3482	A7	3568	A2
2005	A6	2323	C2	2474	A7	2610	B3	2805	B7	2909	A9	3019	A6	3112	C6	3336	C1	3418	A4	3484	A7	3569	A3
2008	A3	2324	A6	2481	A6	2616	B3	2807	A7	2910	B8	3020	A5	3113	C6	3337	A3	3419	A4	3502	A4	3570	A3
2009	A6	2324	B4	2485	A7	2617	B3	2808	B8	2911	B8	3023	A6	3200	B5	3337	C2	3420	A4	3507	A4	3571	A3
2014	A3	2325	A6	2505	B4	2620	B3	2809	B8	2912	A7	3024	A6	3209	B5	3338	C1	3421	A4	3509	A4	3572	A3
2016	A3	2326	B4	2506	A4	2621	B3	2814	A7	2913	B9	3025	B9	3212	B5	3339	C1	3436	A1	3510	A4	3575	A3
2019	A6	2329	C1	2507	B4	2623	C3	2815	A7	2914	B8	3026	B9	3213	B5	3340	C1	3439	A1	3511	A5	3576	A3
2027	A7	2340	A3	2511	B5	2701	C1	2819	A6	2915	B8	3027	B9	3215	B5	3343	A3	3440	A1	3512	A5	3602	B2
2100	C7	2347	A4	2513	B4	2702	C1	2821	A7	2916	B7	3030	B9	3218	B5	3365	A4	3442	A3	3513	A4	3606	B3
2101	C7	2348	B4	2531	B4	2704	A1	2822	B7	2917	B8	3100	C7	3219	B5	3366	A2	3443	A3	3514	A4	3607	B3
2102	C7	2401	A1	2544	A4	2705	B2	2823	A7	2981	A8	3101	C7	3220	B5	3367	A2	3444	A8	3524	B4	3700	BI
2103	C7	2402	A2	2545	A4	2706	B2	2827	C1	3002	A6	3102	C7	3221	B5	3374	A3	3447	A8	3526	A4	3701	A1
2103	C7	2409	A2	2546	A3	2707	B1	2832	A6	3003	A6	3103	C7	3222	B5	3405	A2	3448	A8	3527	A3	3702	B1
2104	C7	2432	A1	2552	A3	2709	B2	2900	B8	3004	A6	3104	C7	3321	C1	3406	A1	3452	A9	3528	A3	3703	A1
2106	C6	2433	A3	2601	C3	2710	B1	2902	B9	3007	A5	3105	C7	3322	C1	3407	A1	3453	A9	3552	A3	3704	C1
2200	A3	2434	A3	2603	B3	2711	C1	2903	B9	3013	B9	3106	C7	3323	C1	3408	A1	3454	A8	3555	A3	3705	B2
2202	B5	2435	A3	2604	B2	2712	B1	2904	A9	3014	B9	3107	C7	3325	C2	3410	A5	3473	A8	3562	A4	3706	B2
2316	B4	2445	A9	2606	B2	2713	A1	2906	B5	3015	B9	3108	C7	3326	C2	3411	A5	3476	A7	3563	A4	3708	C1

3709	B2	3729	B1	3836	B7	3907	B8	5700	A1	6439	A3	6902	A5	7706	B2								
3710	C2	3730	B1	3838	A7	3909	B8	5901	B5	6440	A3	6903	A5	7707	B1								
3711	A1	3800	B6	3842	A7	3913	B9	5903	B8	6441	A3	7100	C7	7708	B1								
3712	B1	3805	B7	3843	A7	3914	B8	5904	A9	6470	A8	7101	C7	7816	A6								
3713	B1	3809	A6	3843	A7	3915	B8	6100	C7	6504	A3	7201	B5	7817	A7								
3714	C1	3810	A6	3846	B8	3919	B9	6101	C7	6508	A3	7322	C2	7905	B8								
3715	B2	3811	A6	3849	A7	3925	B8	6102	C6	6509	A3	7324	C2	7907	B8								
3716	A1	3813	B6	3851	A7	3974	A5	6103	C6	6510	A2	7329	C2	7908	B9								
3717	B2	3816	B7	3853	A5	3978	A9	6104	C6	6511	A3	7330	C1	7909	B9								
3718	B1	3820	B7	3858	A4	4101	C7	6402	A2	6512	A2	7331	C1										
3719	B1	3823	B7	3871	B7	4102	C7	6403	A2	6600	B2	7502	A4										
3720	A1	3823	B7	3873	A7	4320	C1	6405	A1	6700	C1	7503	A4										
3721	B2	3824	B7	3889	B8	4601	B3	6430	A2	6701	C1	7504	A5										
3722	B2	3826	B7	3893	A7	4701	C1	6431	A2	6702	B1	7505	A4										
3723	C2	3828	B7	3894	C1	4702	B1	6432	A1	6703	C1	7700	B1										
3724	B1	3831	B7	3895	C1	4905	A9	6434	A1	6802	A6	7701	B1										
3726	B2	3833	B8	3899	B8	4999	A9	6436	A9	6803	A7	7702	C1										
3727	B2	3833	B7	3900	B8	5001	A6	6437	A8	6900	A4	7703	B1										
3728	B2	3834	B8	3902	B8	5004	B9	6438	A9	6901	A4	7704	B2										



■ PRINTED CIRCUIT BOARD **U model**

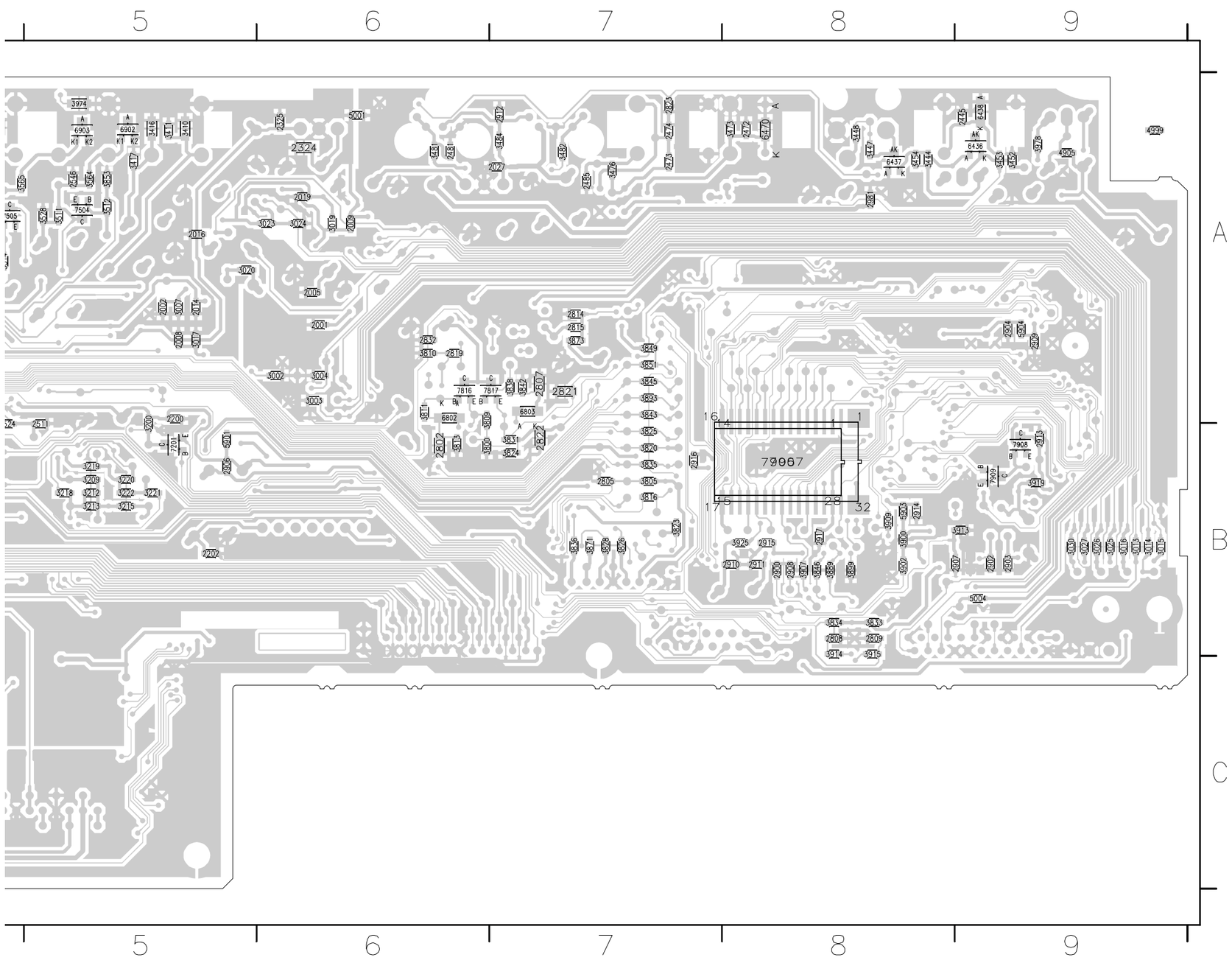
ANALOG P. C. B. **(Part 1 Bottom View)**



■ PRINTED CIRCUIT BOARD

U model

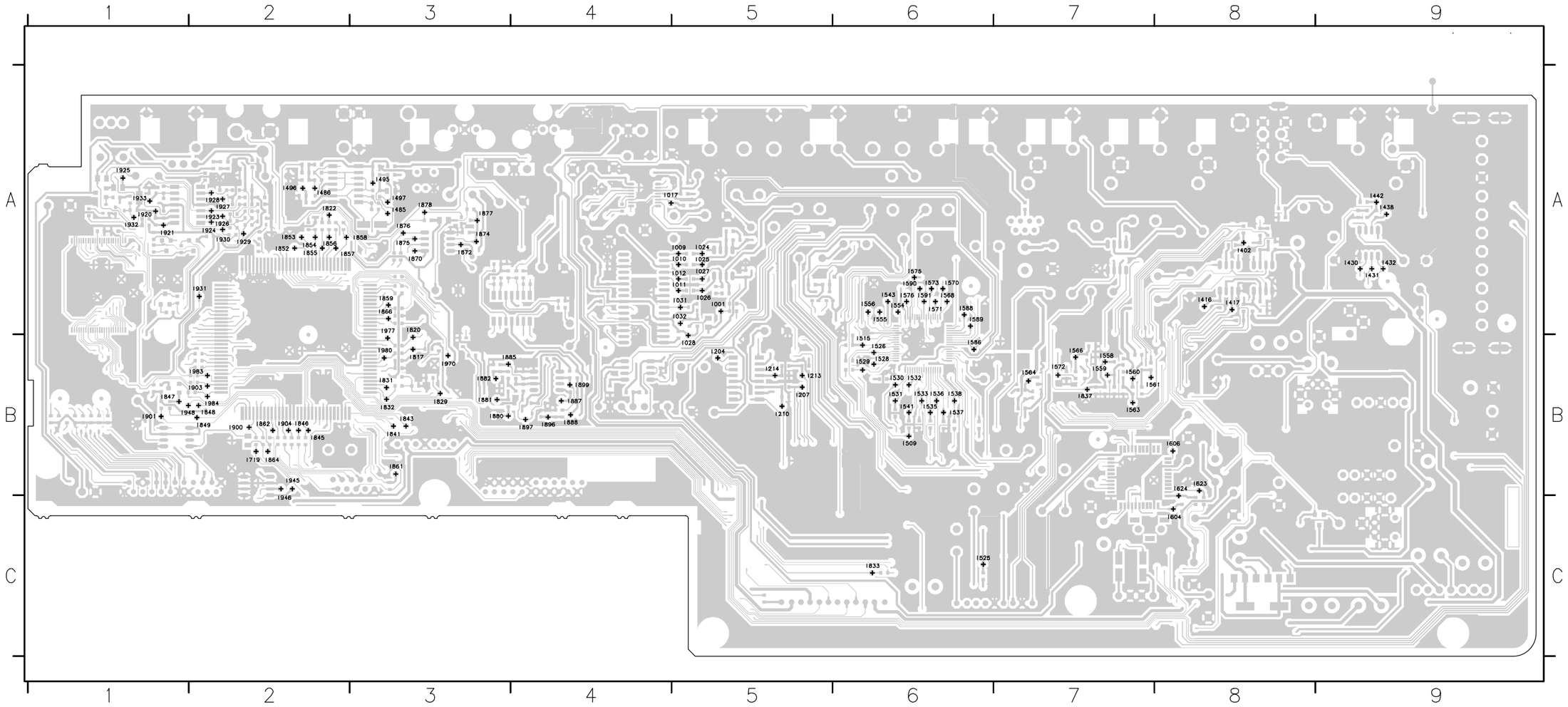
ANALOG P. C. B. **(Part 2 Bottom View)**



■ PRINTED CIRCUIT BOARD **U model**

ANALOG P. C. B. (Testlands Top View)

1001 A5	1024 A5	1032 A5	1402 A8	1438 A9	1497 A3	1529 B6	1536 B6	1555 A6	1563 B7	1572 B7	1589 A6	1624 C8	1831 B3	1845 B2	1853 A2	1859 A3	1872 A3	1880 B3	1896 B4	1904 B2	1926 A2	1932 A1	1977 B3
1009 A5	1025 A5	1204 B5	1416 A8	1442 A9	1509 B6	1530 B6	1537 B6	1556 A6	1564 B7	1573 A6	1590 A6	1719 B2	1832 B3	1846 B2	1854 A2	1861 A3	1874 A3	1881 B3	1897 B4	1920 A1	1927 A2	1933 A1	1980 B3
1010 A5	1026 A5	1207 B5	1417 A8	1485 A3	1515 B6	1531 B6	1538 B6	1558 A6	1566 B7	1575 A6	1591 A6	1817 C8	1833 C6	1847 B1	1855 A2	1862 B2	1875 A3	1882 B3	1899 B4	1921 A1	1928 A2	1945 B2	1983 B2
1011 A5	1027 A5	1210 B5	1430 A9	1486 A2	1525 C6	1532 B6	1541 B6	1559 A6	1568 B7	1576 A6	1604 C8	1820 B3	1837 B7	1848 B2	1856 A2	1864 A3	1876 A3	1885 B3	1900 B2	1923 A2	1929 A2	1946 B2	1984 B2
1012 A5	1028 B5	1213 B5	1431 A9	1495 A3	1526 B6	1533 B6	1543 A6	1560 B7	1570 A6	1577 A6	1606 B8	1822 A2	1841 B3	1849 B2	1857 A2	1866 A3	1877 A3	1887 B3	1901 B2	1924 A2	1930 A2	1948 B1	
1017 A4	1031 A5	1214 B5	1432 A9	1496 A2	1528 B6	1535 B6	1554 A6	1561 B7	1571 A6	1588 A6	1623 B8	1829 A2	1843 B3	1852 A2	1858 A2	1870 A3	1878 A3	1888 B4	1903 B2	1925 A1	1931 A2	1970 B3	



■ PRINTED CIRCUIT BOARD

U model

ANALOG P. C. B. (Testlands Bottom View)

F0001 B9 F0002 B9 F0003 B9 F0005 B9 F0007 B9 F0009 B9 F0011 B9 F0012 B9 F0014 B8 F0016 B8 F0017 B9 F010 A4 F011 A4 F012 B8 F013 A7 F014 B8 F1001 C7 F1002 C6

F1005 C7 F1007 C7 F1008 C7 F1101 C7 F1103 C7 F1104 C7 F1105 C7 F1106 C7 F1107 C6 F1108 C6 F1109 C6 F303 B1 F3201 C1 F3202 C1 F3203 C1 F3204 C1 F3205 C1 F3206 C1

F3207 C1 F330 A8 F337 A2 F338 A2 F339 A6 F340 B6 F341 B6 F342 A8 F4102 A8 F4103 A9 F4202 A7 F4203 A7 F4204 A6 F4205 A7 F509 A4 F510 A4 F5101 A5 F5103 A5

F5104 A4 F5105 A4 F511 A1 F512 A5 F513 A5 F5201 A1 F5202 A1 F5205 A1 F5301 C4 F5303 C4 F5304 C4 F5306 C3 F5307 C3 F5309 C3 F5401 B7 F5402 B7 F5405 B7

F5407 B6 F5409 B6 F5410 B6 F5412 B6 F5414 B6 F5416 B6 F5418 B6 F5420 B6 F5421 A5 F5422 B6 F5501 A2 F5502 A2 F5504 A2 F5801 A2 F5802 A2 F5805 A2 F5806 A3 F5901 A3 F5902 A3

F5905 A3 F5906 C3 F6001 C3 F6002 C3 F6004 C3 F6101 A4 F6102 A3 F6105 A3 F6106 A3 F6202 A3 F6204 A3 F6206 A3 F700 A1 F701 C1 F702 A1 F703 C1 F705 A1 F800 B7

F8001 B7 F8002 B3 F8003 C5 F8004 B7 F8005 B7 F8006 B7 F8007 B7 F8008 B7 F810 A5 F811 B7 F8110 C4 F8111 C4 F8112 C5 F812 A8 F813 A9 F814 A9 F8201 B8 F8202 B8 F910 B7

F8102 C5 F8103 C5 F8104 C5 F8105 C5 F8106 B8 F8107 C4 F8108 C4 F8109 C4 F811 B7

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F930 B8 F931 A8 F932 A8 F933 B8 F9330 C1 F9332 C1 F9333 C1 F9336 B7 F9338 C2 F9341 C2 F9342 C2 F9344 C2 F9345 C2 F9346 C1 F9349 C4 F9350 C4

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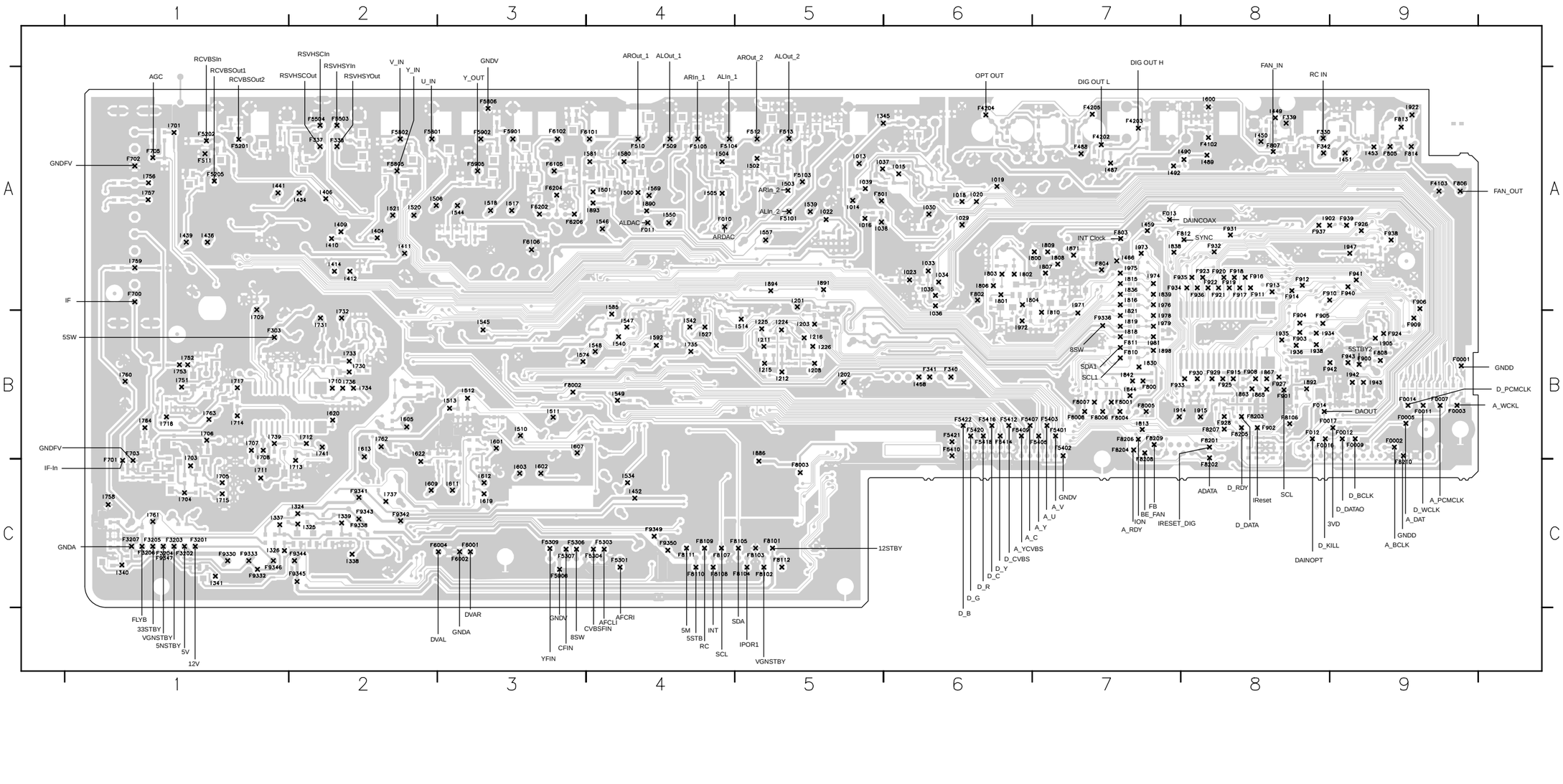
I705 C1 I706 B1 I707 B1 I708 B1 I709 A1 I710 B2 I711 C1 I712 B2 I713 C2 I714 B1 I715 C1 I717 B1 I718 B1 I730 B2 I731 B2 I732 B2 I733 B2 I734 B2

I735 B4 I736 B2 I737 C2 I739 B1 I741 B2 I751 B1 I752 B1 I753 B1 I756 A1 I757 A1 I758 C1 I759 A1 I760 B1 I761 C1 I762 B2 I763 B1 I764 B1 I800 A7

I801 A6 I802 A6 I803 A6 I804 A6 I806 A6 I807 A7 I808 A7 I809 A7 I810 B7 I813 B7 I815 A7 I816 A7 I818 B7 I819 B7 I821 B7 I830 B7 I836 A7 I838 A7

I839 A7 I842 B7 I844 B7 I846 B7 I863 B8 I865 B8 I867 B8 I871 A7 I886 C5 I890 A4 I891 A5 I892 B8 I893 A4 I894 A5 I898 B7 I902 A8 I905 B9 I914 B7 I915 B8

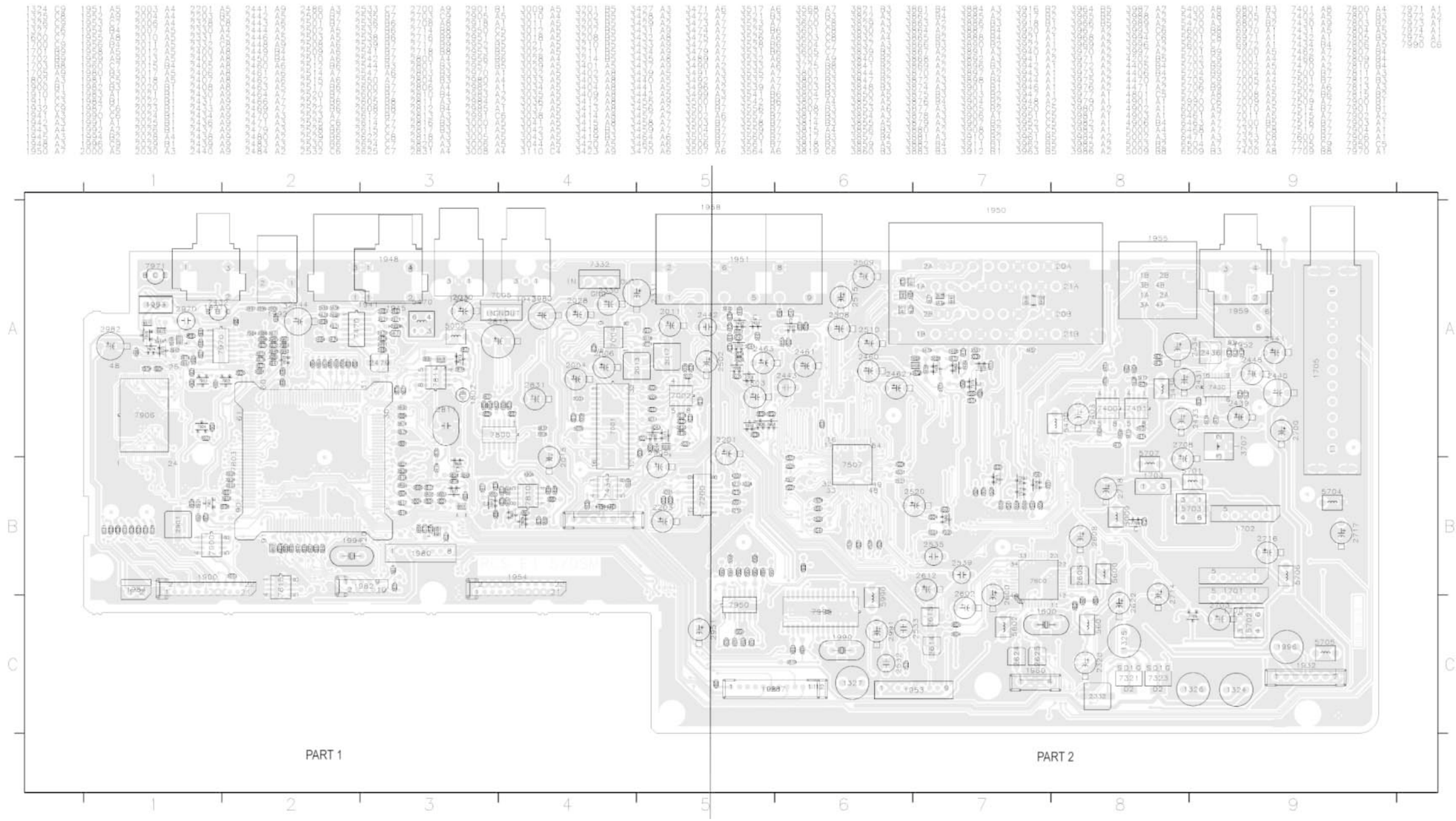
I922 A9 I934 B8 I935 B8 I936 B8 I938 B8 I942 B9 I943 B9 I947 A9 I971 B7 I972 B6 I973 A6 I974 A7 I975 A7 I976 A7 I978 A7 I979 A7 I981 B7



■ PRINTED CIRCUIT BOARD

A, B, G model

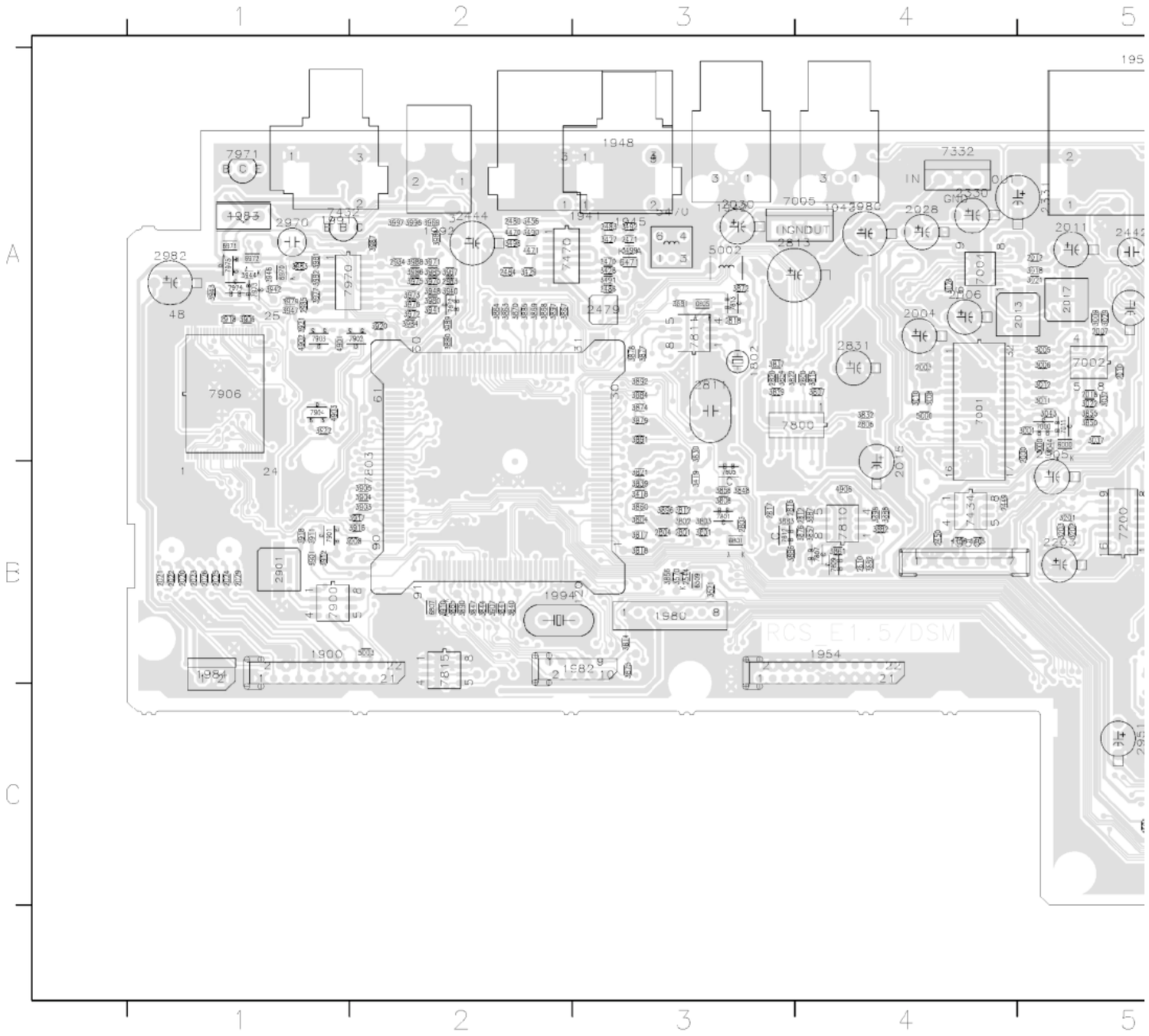
ANALOG P. C. B. **(Overview Top View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

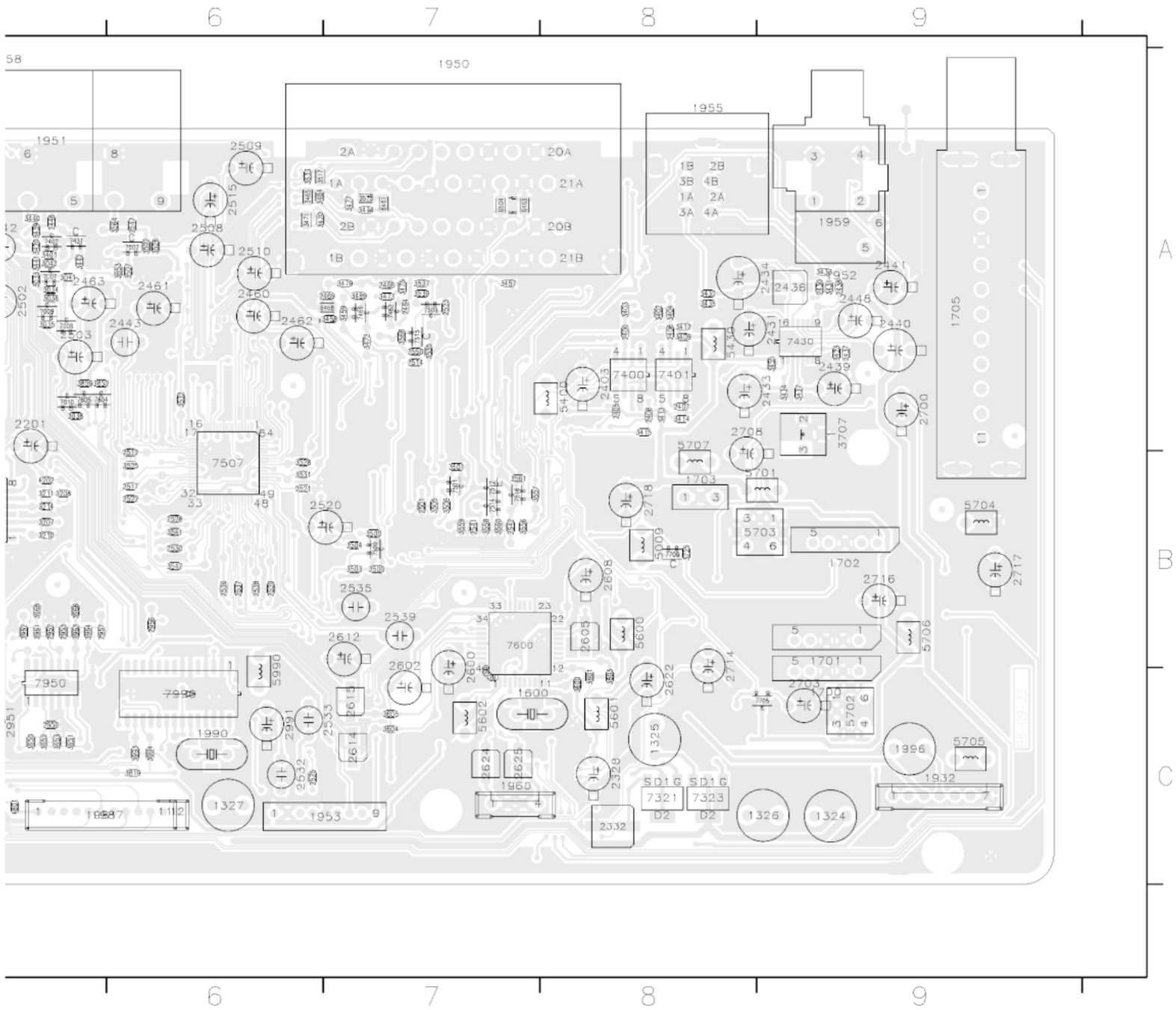
ANALOG P. C. B. **(Part 1 Top View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

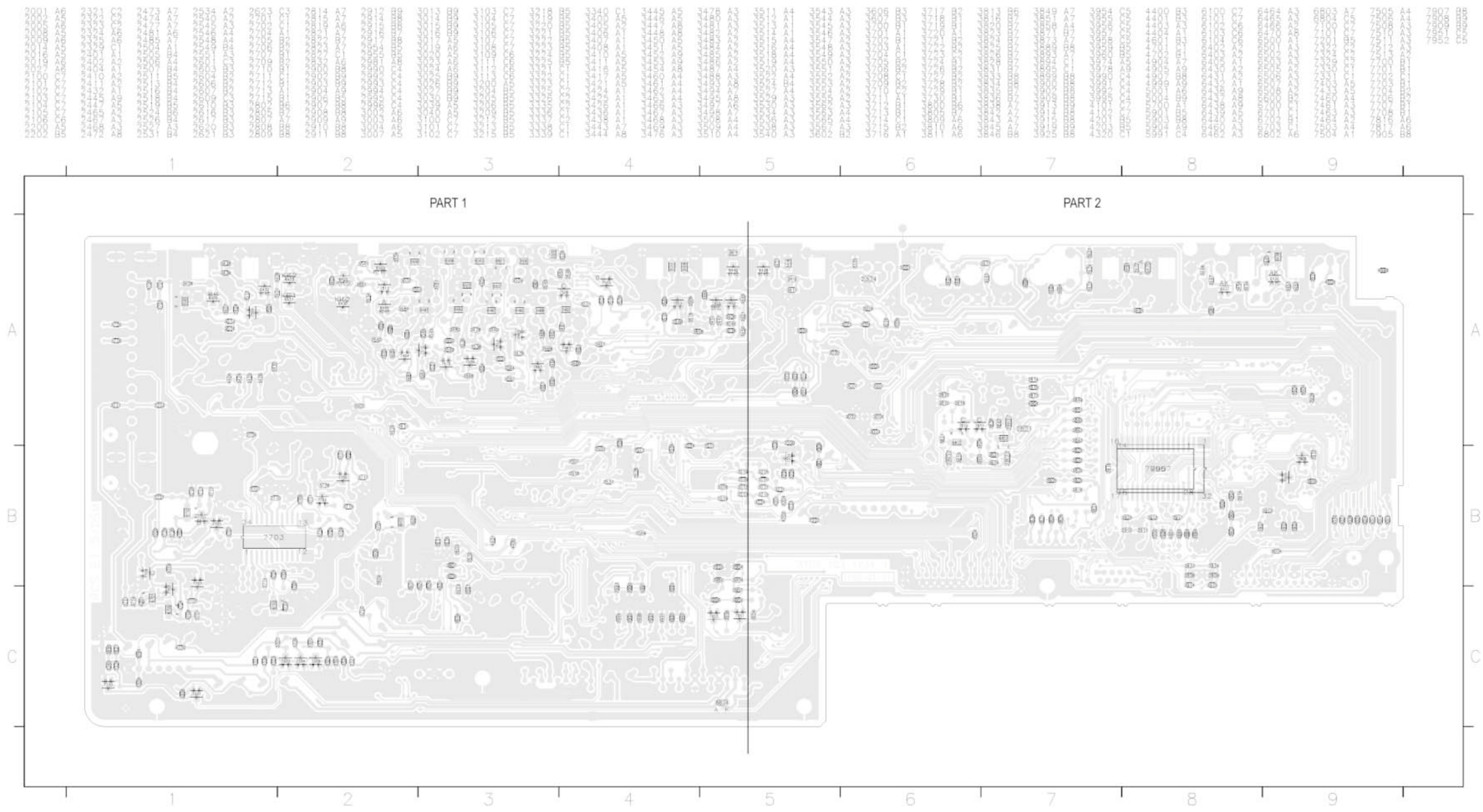
ANALOG P. C. B. **(Part 2 Top View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

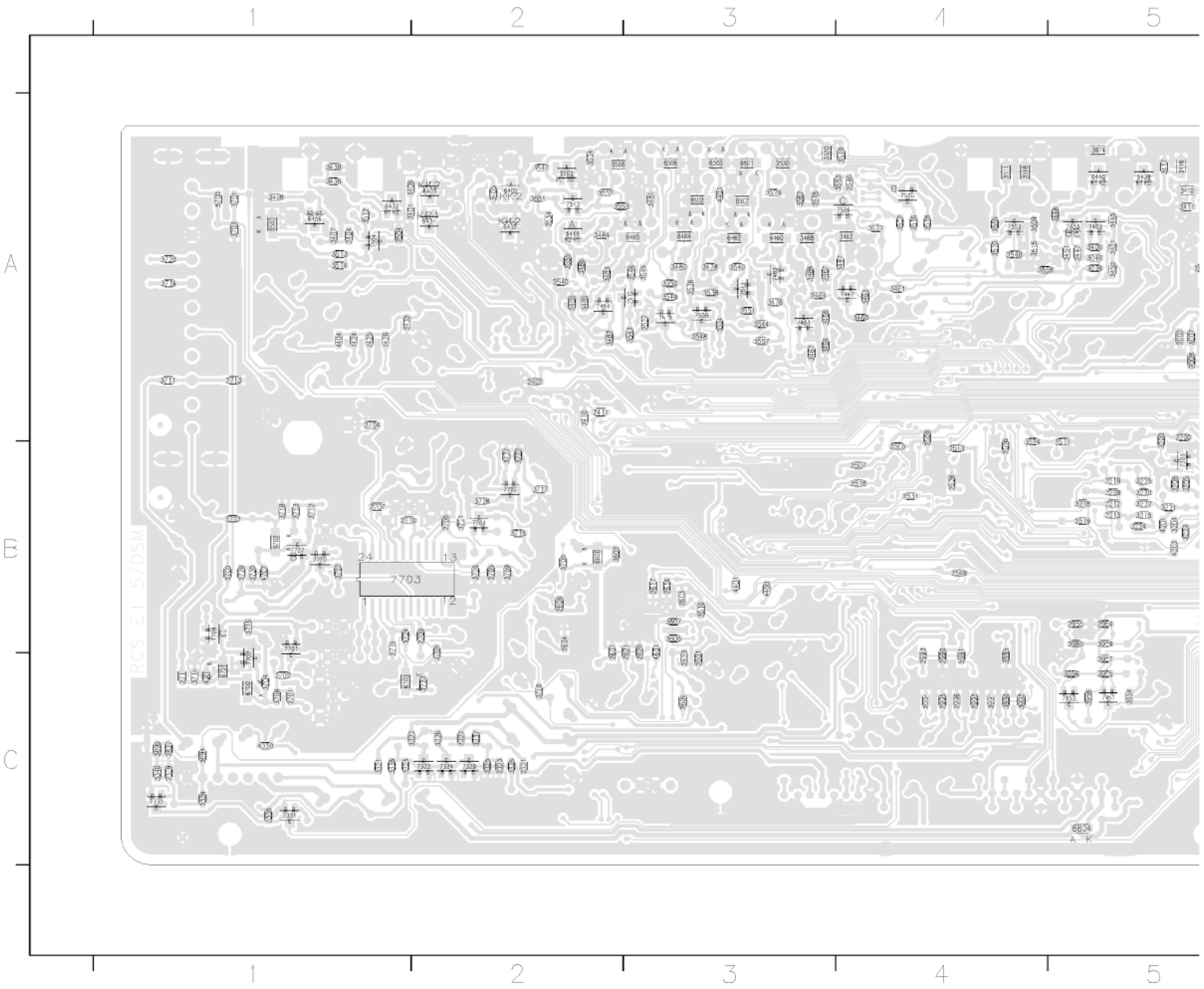
ANALOG P. C. B. **(Overview Bottom View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

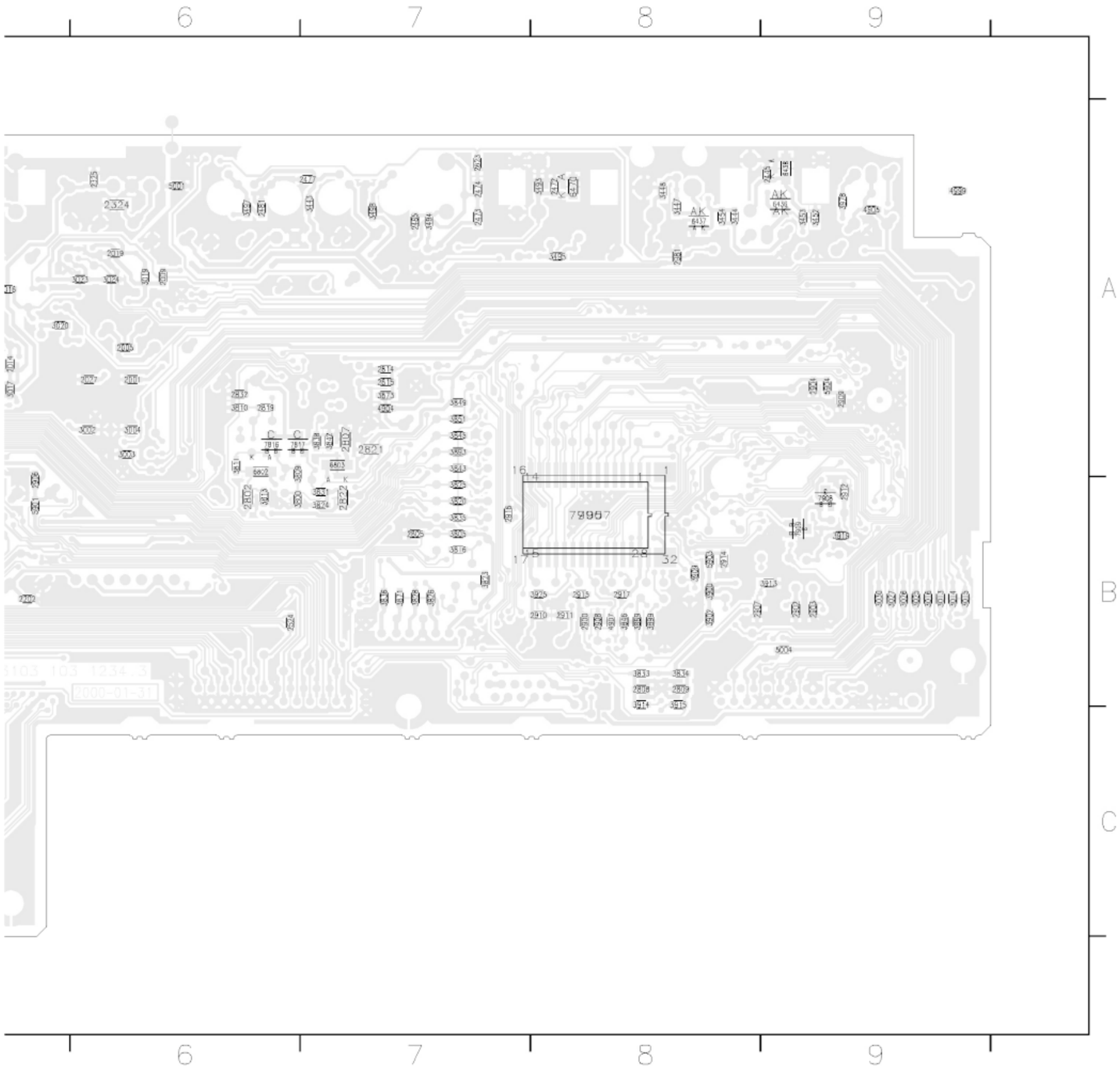
ANALOG P. C. B. **(Part 1 Bottom View)**



■ PRINTED CIRCUIT BOARD

A, B, G model

ANALOG P. C. B. **(Part 2 Bottom View)**

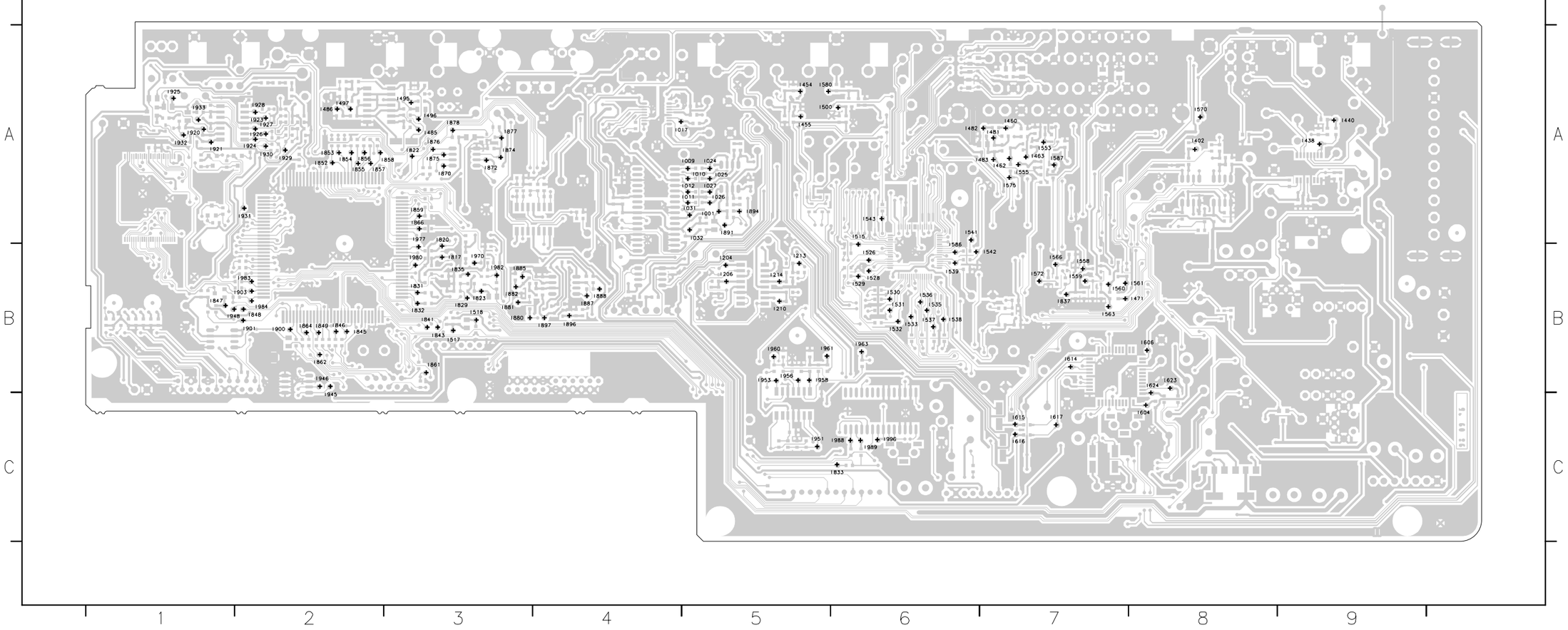


■ PRINTED CIRCUIT BOARD

A, B, G model

ANALOG P. C. B. (Testlands Top View)

1001 A5 1009 A5 1010 A5 1011 A5 1012 A5 1017 A4
1024 A5 1025 A5 1026 A5 1027 A5 1031 A5 1032 A5
1204 B5 1206 B5 1210 B5 1213 B5 1214 B5 1402 A8
1438 A9 1440 A9 1454 A5 1455 A5 1460 A7 1462 A7
1463 A7 1471 B7 1481 A7 1482 A7 1483 A7 1485 A3
1486 A2 1495 A3 1496 A3 1497 A2 1500 A6 1515 B6
1517 B3 1518 B3 1526 B6 1528 B6 1529 B6 1530 B6
1531 B6 1532 B6 1533 B6 1535 B6 1536 B6 1537 B6
1538 B6 1539 B6 1541 A6 1542 B6 1543 A6 1553 A7
1555 B6 1558 B7 1559 B7 1560 B7 1561 B7 1563 B7
1566 B7 1570 A8 1572 B7 1575 A7 1580 A5 1586 B6
1587 A7 1604 C8 1606 B8 1614 B7 1615 C7 1616 C7
1617 C7 1623 B8 1624 C8 1817 B3 1820 B3 1822 A3
1823 B3 1829 B3 1831 B3 1832 B3 1833 C6 1835 B3
1837 B7 1841 B5 1843 B5 1845 B2 1846 B2 1847 B1
1848 B2 1849 B2 1850 A2 1851 A2 1852 A2 1853 A2
1854 A2 1855 A2 1856 A2 1857 A2 1858 A2 1859 A2
1861 B2 1862 B2 1864 B2 1866 A3 1870 A3 1872 A3
1874 A3 1875 A3 1876 A3 1877 A3 1878 A3 1880 B3
1881 B3 1882 B3 1885 B3 1887 B4 1888 B4 1891 A5
1894 A5 1896 B4 1897 B4 1900 B2 1901 B2 1903 B2
1920 A1 1921 A1 1923 A2 1924 A2 1925 A1 1926 A2
1927 A2 1928 A2 1929 A2 1930 A2 1931 A2 1932 A1
1933 A1 1945 B2 1946 B2 1948 B1 1951 C5 1953 B5
1956 B5 1958 B5 1960 B5 1961 B5 1963 B6 1970 B3
1977 B3 1980 B3 1982 B3 1983 B2 1984 B2 1988 C6
1989 C6 1996 C6



■ PRINTED CIRCUIT BOARD

A, B, G model

ANALOG P. C. B. (Testlands Bottom View)

F0001 B9 F0002 B9 F0003 B9 F0004 B9 F0005 B9 F0006 B8 F0007 B9 F0008 B9 F0009 B9 F0010 B9 F0011 B9 F0012 B9 F0013 B9 F0014 B8 F0015 B8 F0016 B8 F0017 B9 F0101 A5 F0102 B8 F0103 A7 F0104 B8 F0105 C7 F0106 C7 F0107 C7 F0108 C7 F0109 C7 F0110 C7 F0111 C7 F0112 C7 F1001 C7 F1002 C7 F1003 C7 F1004 C7 F1005 C7 F1007 C7 F1008 C7 F1101 C7 F1103 C7 F1104 C7 F1105 C7 F1106 C7 F1107 C6 F1108 C6 F1109 C6 F1110 C6 F1111 C6 F1112 C6 F3001 C1 F3002 C1 F3003 C1 F3004 C1 F3005 C1 F3006 C1 F3007 C5 F3008 A8 F3009 A8 F3010 A8 F3011 A8 F3012 A8 F3013 A8 F3014 A8 F3015 A8 F3016 A8 F3017 A8 F3018 A8 F3019 A8 F3020 A8 F3021 A8 F3022 A8 F3023 A8 F3024 A8 F3025 A8 F3026 A8 F3027 A8 F3028 A8 F3029 A8 F3030 A8 F3031 A8 F3032 A8 F3033 A8 F3034 A8 F3035 A8 F3036 A8 F3037 A8 F3038 A8 F3039 A8 F3040 A8 F3041 A8 F3042 A8 F3043 A8 F3044 A8 F3045 A8 F3046 A8 F3047 A8 F3048 A8 F3049 A8 F3050 A8 F3051 A8 F3052 A8 F3053 A8 F3054 A8 F3055 A8 F3056 A8 F3057 A8 F3058 A8 F3059 A8 F3060 A8 F3061 A8 F3062 A8 F3063 A8 F3064 A8 F3065 A8 F3066 A8 F3067 A8 F3068 A8 F3069 A8 F3070 A8 F3071 A8 F3072 A8 F3073 A8 F3074 A8 F3075 A8 F3076 A8 F3077 A8 F3078 A8 F3079 A8 F3080 A8 F3081 A8 F3082 A8 F3083 A8 F3084 A8 F3085 A8 F3086 A8 F3087 A8 F3088 A8 F3089 A8 F3090 A8 F3091 A8 F3092 A8 F3093 A8 F3094 A8 F3095 A8 F3096 A8 F3097 A8 F3098 A8 F3099 A8 F3100 A8 F3101 A8 F3102 A8 F3103 A8 F3104 A8 F3105 A8 F3106 A8 F3107 A8 F3108 A8 F3109 A8 F3110 A8 F3111 A8 F3112 A8 F3113 A8 F3114 A8 F3115 A8 F3116 A8 F3117 A8 F3118 A8 F3119 A8 F3120 A8 F3121 A8 F3122 A8 F3123 A8 F3124 A8 F3125 A8 F3126 A8 F3127 A8 F3128 A8 F3129 A8 F3130 A8 F3131 A8 F3132 A8 F3133 A8 F3134 A8 F3135 A8 F3136 A8 F3137 A8 F3138 A8 F3139 A8 F3140 A8 F3141 A8 F3142 A8 F3143 A8 F3144 A8 F3145 A8 F3146 A8 F3147 A8 F3148 A8 F3149 A8 F3150 A8 F3151 A8 F3152 A8 F3153 A8 F3154 A8 F3155 A8 F3156 A8 F3157 A8 F3158 A8 F3159 A8 F3160 A8 F3161 A8 F3162 A8 F3163 A8 F3164 A8 F3165 A8 F3166 A8 F3167 A8 F3168 A8 F3169 A8 F3170 A8 F3171 A8 F3172 A8 F3173 A8 F3174 A8 F3175 A8 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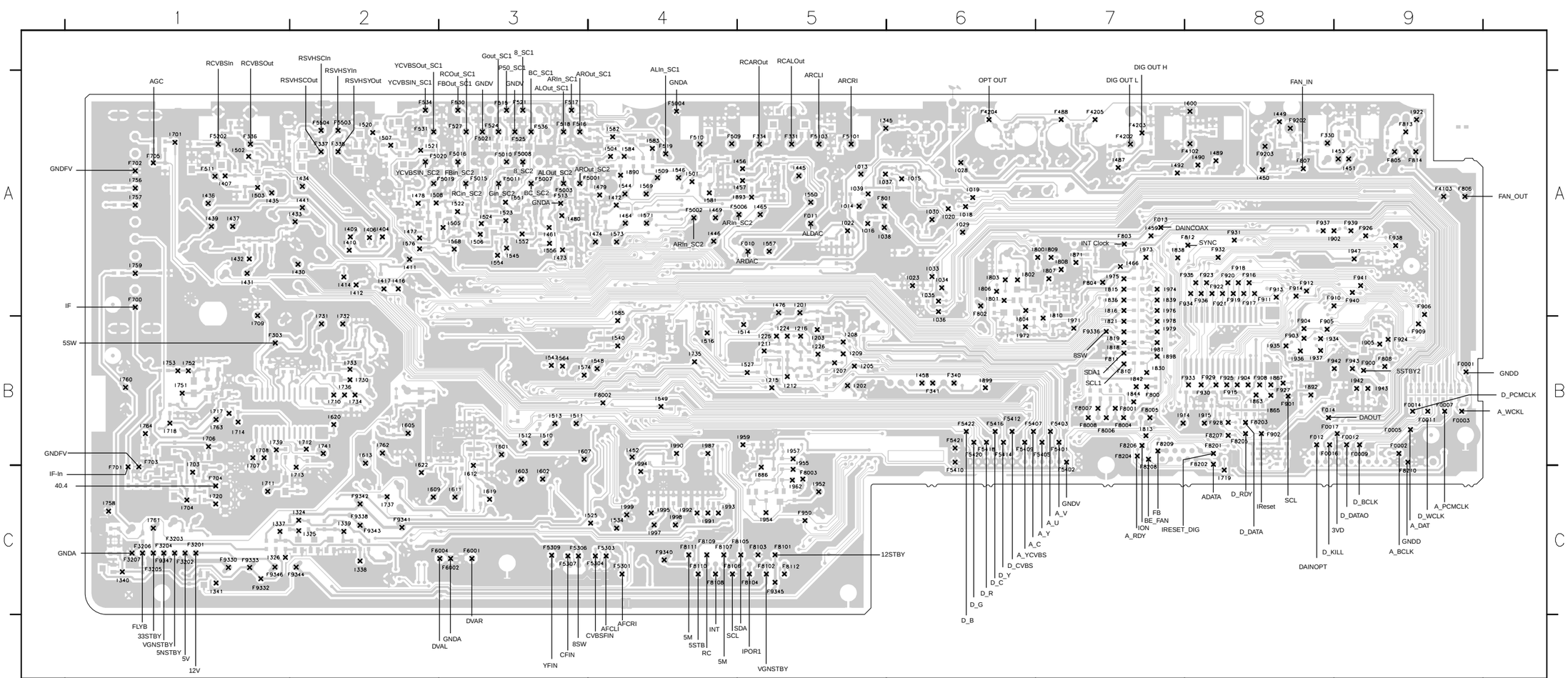


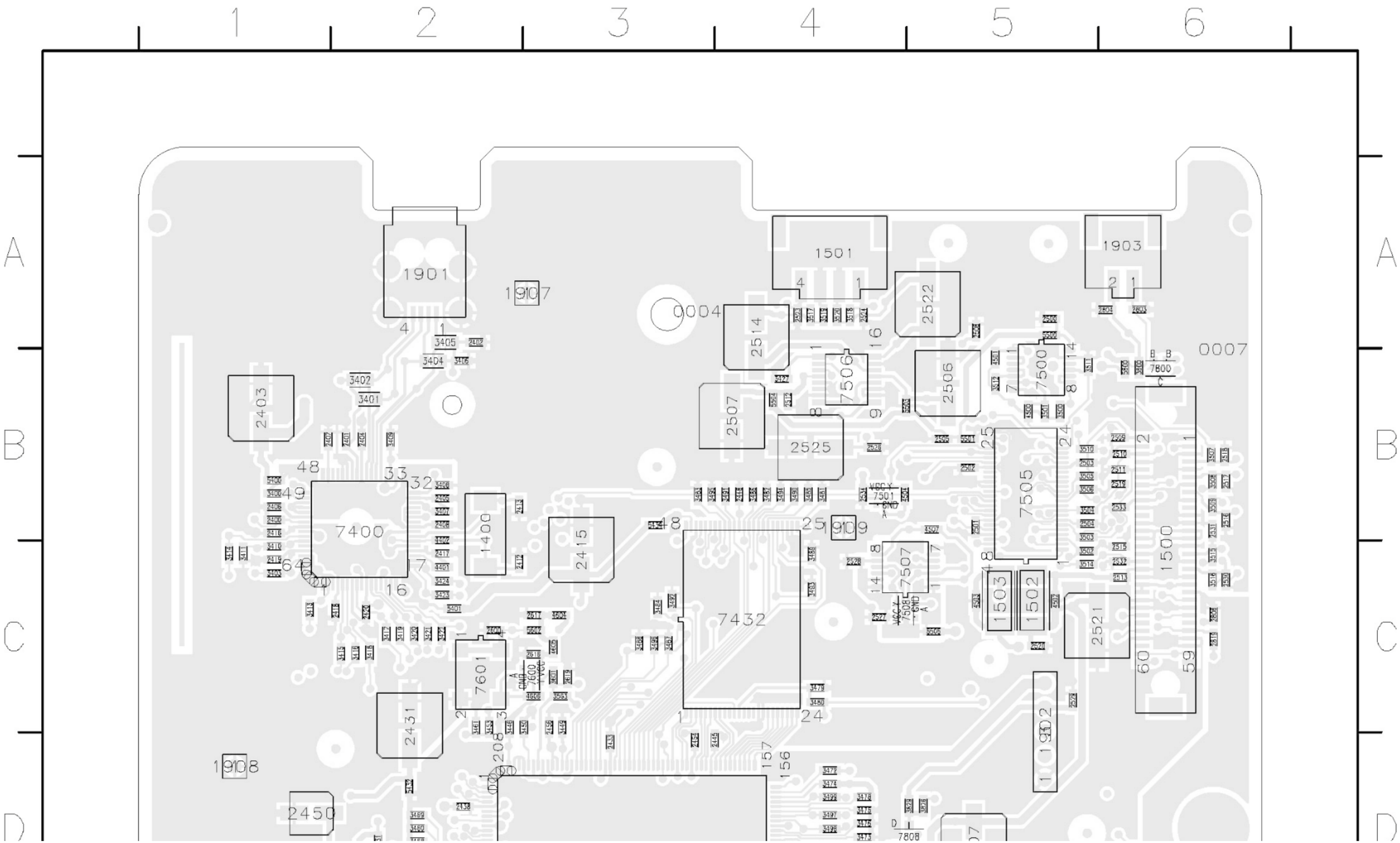
■ PRINTED CIRCUIT BOARD

DVIO P. C. B. **(Overview Top View)**

1400	B2	2503	B5	2810	E5	3450	C3	3511	B5	3800	B6	5501	B5
1500	C6	2504	B5	2811	F5	3451	F2	3512	B5	3801	F5	5503	B4
1501	A4	2505	B5	2812	D4	3452	G3	3514	C5	3802	E6	5504	B4
1502	C5	2506	B5	2813	E6	3453	C2	3515	C6	3803	E4	5505	C5
1503	C5	2507	B4	2814	E6	3454	E2	3516	C6	3804	E4	5600	G4
1800	F5	2508	A5	2816	E4	3455	E2	3517	A4	3805	E4	5601	F4
1901	A2	2509	B6	2817	E4	3456	E2	3518	A4	3806	E4	5602	C3
1902	C5	2510	B6	2818	D4	3457	D2	3519	A4	3807	E4	5603	F5
1903	A6	2511	B6	2819	C6	3458	D2	3520	A4	3808	F5	5800	B6
1904	F6	2512	B4	2820	F5	3459	D2	3530	G3	3809	G6	5801	D5
1905	F4	2513	C6	2821	F5	3460	D2	3531	F2	3810	E4	5802	D6
1906	G5	2514	A4	2822	D6	3461	C2	3532	F2	3811	E4	6801	G5
1907	A3	2515	C6	3400	B1	3462	E2	3533	F2	3812	E4	6802	G5
1908	D1	2516	B6	3401	B2	3463	E2	3534	G3	3813	E4	6803	F6
1909	B4	2517	B6	3402	B2	3464	E2	3535	F2	3814	F5	6804	E6
2400	B1	2518	B6	3403	C1	3465	D2	3536	G3	3815	G5	7400	B2
2401	B2	2519	B6	3404	B2	3466	D2	3537	F2	3816	G5	7430	F2
2402	A2	2520	C5	3405	A2	3467	D2	3538	G3	3817	E6	7431	D3
2403	B1	2521	C5	3406	B2	3468	D2	3539	F2	3818	E6	7432	C4
2404	B2	2522	A5	3407	B2	3469	D2	3540	G3	3819	E6	7433	D1
2405	B2	2523	A4	3408	B2	3470	E4	3541	F2	3820	E6	7500	B5
2406	B1	2524	A4	3409	B2	3471	E2	3542	F3	3821	G5	7501	B4
2407	B1	2525	B4	3410	C1	3472	D4	3543	F2	3822	E5	7505	B5
2408	B2	2526	B4	3411	C1	3473	D4	3544	E3	3823	G5	7506	B4
2412	C2	2527	C4	3413	C1	3474	D4	3545	F2	3824	G5	7507	C4
2413	B2	2528	C4	3414	C1	3475	D4	3546	F3	3825	E4	7508	C4
2415	C3	2529	C5	3415	C2	3476	D4	3547	F2	3826	D5	7600	C3
2416	B1	2530	C6	3416	C2	3477	D4	3548	E3	3827	D4	7601	C2
2417	C2	2531	B6	3417	C2	3478	D4	3549	F2	3828	F5	7602	F4
2418	C2	2532	C6	3418	C2	3479	C4	3550	F3	3829	D5	7604	F4
2419	C1	2533	B6	3419	C2	3480	C4	3551	F3	3831	E5	7605	F4
2420	C2	2534	B4	3420	C2	3481	B4	3552	E3	3832	E5	7606	F4
2431	C2	2600	C2	3421	C2	3482	B4	3553	F3	3833	E4	7608	F4
2432	E2	2601	G3	3422	C2	3483	B3	3554	G3	3834	E4	7800	B6
2433	D3	2602	F3	3423	C2	3484	C3	3555	F3	3835	F6	7801	G5
2434	E4	2603	F4	3424	C2	3485	B4	3556	F3	3836	G6	7802	E5
2435	D4	2604	F4	3425	E4	3486	B4	3557	E3	3837	D5	7803	E6
2436	G2	2605	F4	3426	E3	3487	C3	3558	F3	3838	D6	7804	E6
2437	E2	2606	F4	3427	B4	3488	C3	3559	G3	3839	F6	7805	E6
2438	D2	2607	F4	3428	E3	3489	C4	3560	G3	4401	C2	7806	G6
2439	G3	2608	F5	3429	E4	3490	B4	3561	G2	4402	B2	7807	D4
2440	E3	2609	F4	3430	F2	3491	B4	3562	E2	4500	B5	7808	D5
2441	F2	2610	F4	3431	F2	3492	C3	3563	C3	4501	B5	7809	F5
2442	E3	2611	F4	3432	F2	3493	C4	3564	E4	4502	C5	7810	F6
2443	E3	2612	F4	3433	F2	3494	B4	3600	F3	4503	C5	7811	F6
2444	F2	2613	F4	3434	F2	3495	B3	3601	C3	4504	B4		
2445	D3	2614	F3	3435	F2	3496	C3	3602	F4	4507	B5		
2446	G2	2615	F3	3436	F2	3497	D4	3603	F5	4602	F3		
2447	G2	2616	C3	3437	F2	3498	D4	3604	F4	4603	F4		
2448	B4	2617	C3	3438	F2	3499	D4	3605	F4	4604	C3		
2449	D2	2618	F4	3439	F2	3500	B5	3606	F4	4605	C3		
2450	D1	2619	C3	3440	F2	3501	B5	3607	F3	4606	C3		
2451	E3	2801	F5	3441	F3	3502	C5	3608	F3	4608	E4		
2452	E4	2802	F5	3442	F3	3503	B5	3609	F4	4609	E4		
2453	D2	2803	A6	3443	F3	3504	B5	3610	F4	5400	B1		
2454	D3	2804	A6	3444	F3	3505	B5	3612	F4	5401	C2		
2455	D2	2805	F5	3445	F3	3506	B5	3613	F4	5431	D2		
2456	C3	2806	C6	3446	C2	3507	B6	3614	F4	5432	D2		
2500	A5	2807	D5	3447	F3	3508	B6	3616	F5	5433	G2		
2501	B5	2808	D5	3448	G2	3509	B6	3617	F5	5434	B3		
2502	B5	2809	F5	3449	C3	3510	B5	3618	F4	5500	A5		

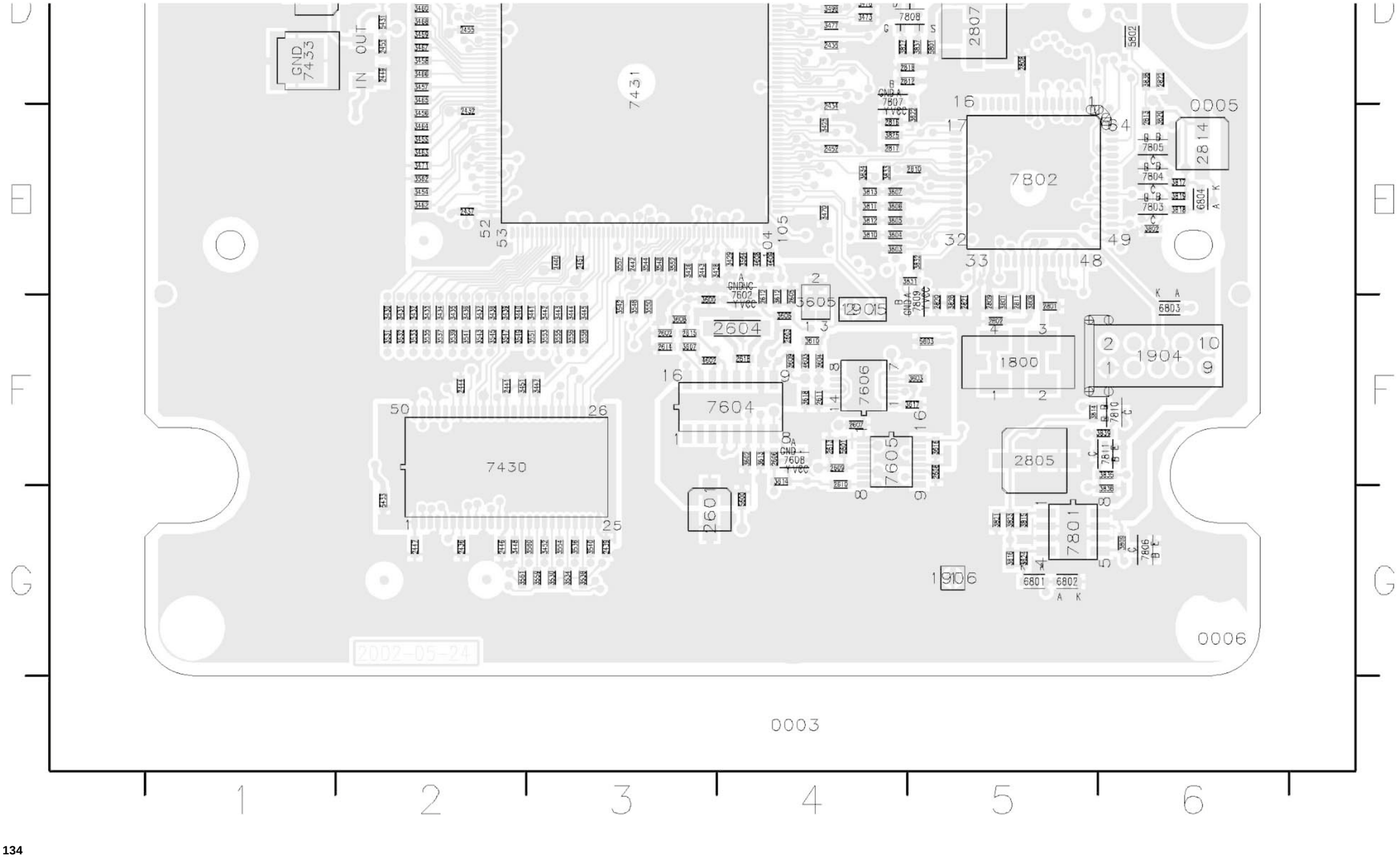
■ PRINTED CIRCUIT BOARD

DVIO P. C. B. **(Part 1 Top View)**



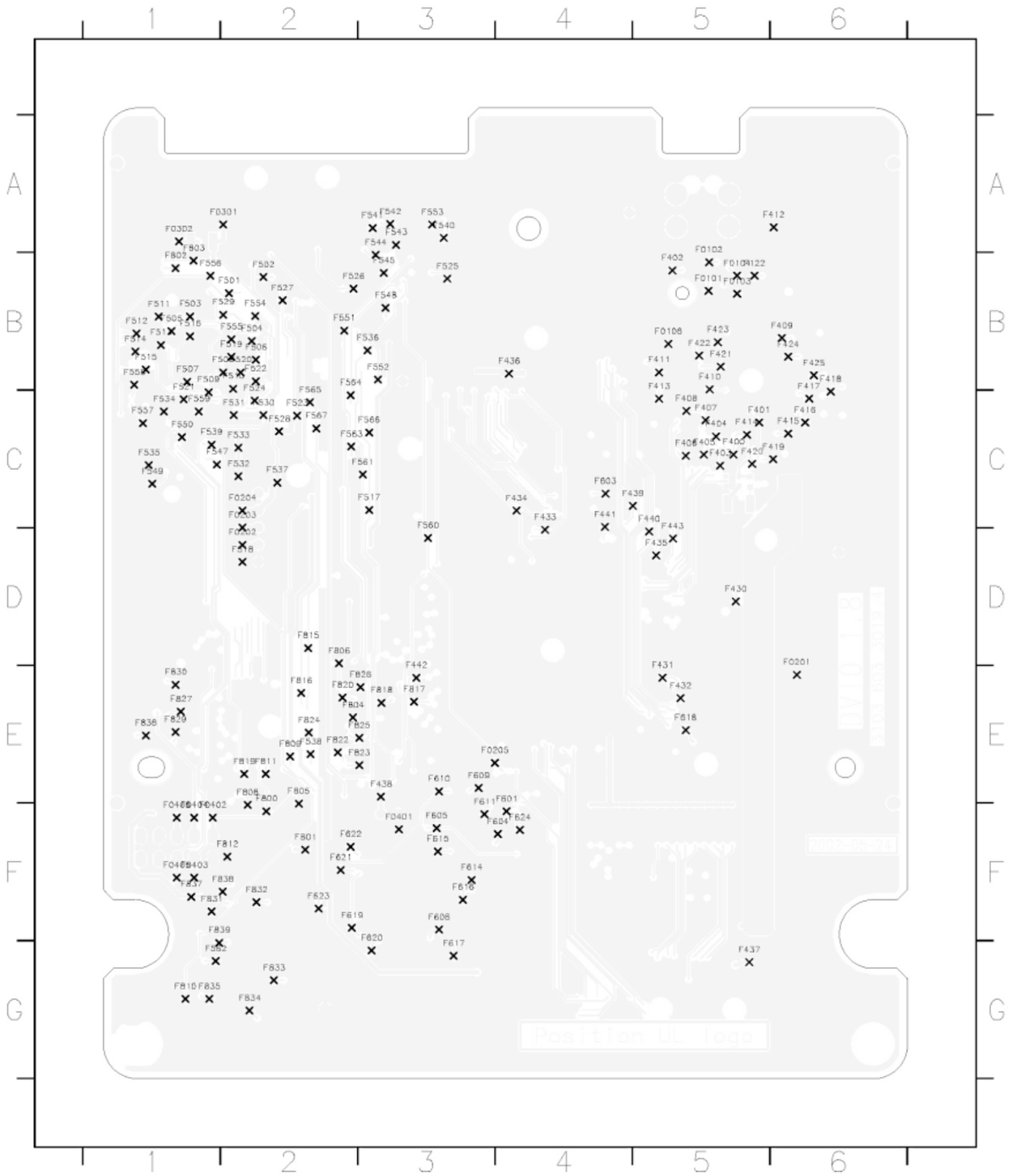
■ PRINTED CIRCUIT BOARD

DVIO P. C. B. **(Part 2 Top View)**



■ PRINTED CIRCUIT BOARD

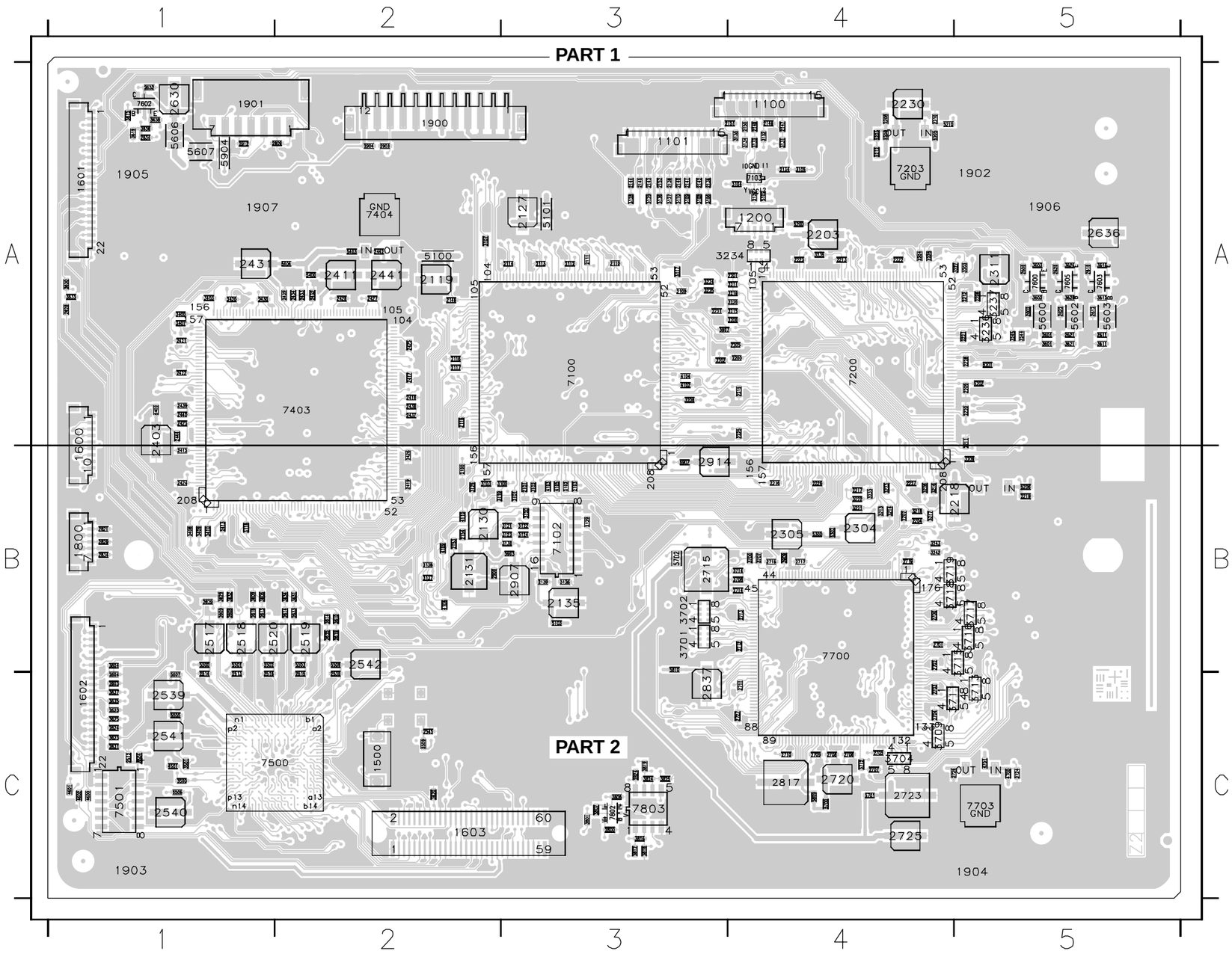
DVIO P. C. B. **(Testlands Bottom View)**



F0101	B5	F503	B1	F565	C2				
F0102	B5	F504	B2	F566	C3				
F0103	B5	F505	B1	F567	C2				
F0104	B5	F506	B2	F601	F4				
F0106	B5	F507	B1	F603	C4				
F0201	E6	F508	B2	F604	F4				
F0202	D2	F509	C1	F605	F3				
F0203	C2	F510	B2	F606	F3				
F0204	C2	F511	B1	F609	E3				
F0205	E3	F512	B1	F610	E3				
F0301	A2	F513	B1	F611	F3				
F0302	A1	F514	B1	F614	F3				
F0401	F3	F515	B1	F615	F3				
F0402	F1	F516	B1	F616	F3				
F0403	F1	F517	C3	F617	G3				
F0404	F1	F518	D2	F618	E5				
F0405	F1	F519	B2	F619	F2				
F0406	F1	F520	B2	F620	G3				
F122	B5	F521	C1	F621	F2				
F400	C5	F522	B2	F622	F2				
F401	C5	F523	C2	F623	F2				
F402	B5	F524	C2	F624	F4				
F403	C5	F525	B3	F800	F2				
F404	C5	F526	B2	F801	F2				
F405	C5	F527	B2	F802	B1				
F406	C5	F528	C2	F803	B1				
F407	C5	F529	B2	F804	E2				
F408	C5	F530	C2	F805	F2				
F409	B6	F531	C2	F806	D2				
F410	B5	F532	C2	F808	F2				
F411	B5	F533	C2	F809	E2				
F412	A6	F534	C1	F810	G1				
F413	C5	F535	C1	F811	E2				
F414	C5	F536	B3	F812	F2				
F415	C6	F537	C2	F815	D2				
F416	C6	F538	E2	F816	E2				
F417	C6	F539	C1	F817	E3				
F418	C6	F540	A3	F818	E3				
F419	C6	F541	A3	F819	E2				
F420	C5	F542	A3	F820	E2				
F421	B5	F543	A3	F822	E2				
F422	B5	F544	B3	F823	E3				
F423	B5	F545	B3	F824	E2				
F424	B6	F547	C1	F825	E3				
F425	B6	F548	B3	F826	E3				
F430	D5	F549	C1	F827	E1				
F431	E5	F550	C1	F829	E1				
F432	E5	F551	B2	F830	E1				
F433	D4	F552	B3	F831	F1				
F434	C4	F553	A3	F832	F2				
F435	D5	F554	B2	F833	G2				
F436	B4	F555	B2	F834	G2				
F437	G5	F556	B1	F835	G1				
F438	E3	F557	C1	F836	E1				
F439	C5	F558	B1	F837	F1				
F440	D5	F559	C1	F838	F2				
F441	C4	F560	D3	F839	G1				
F442	E3	F561	C3						
F443	D5	F562	G1						
F501	B2	F563	C2						
F502	B2	F564	C2						

■ PRINTED CIRCUIT BOARD

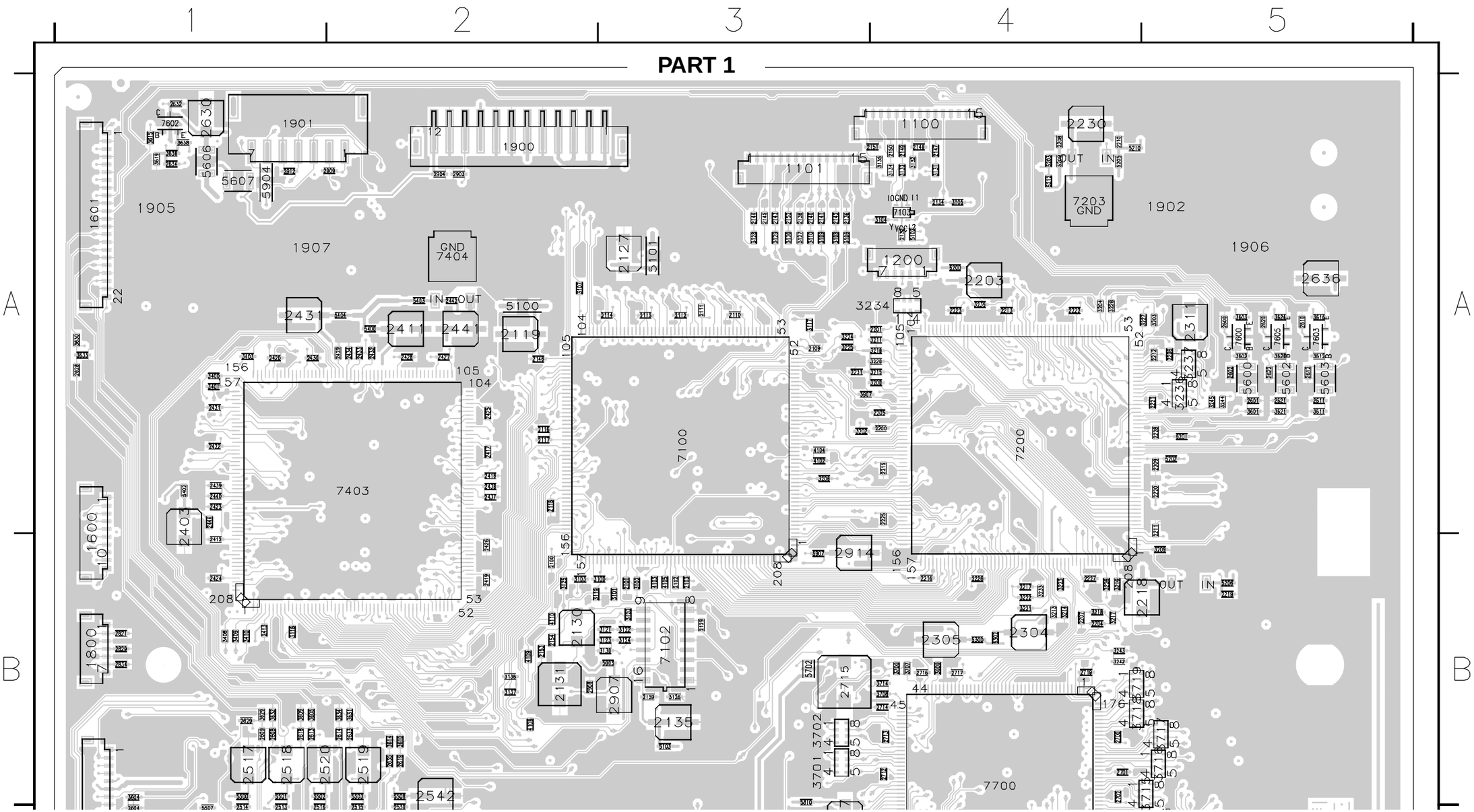
DIGITAL P. C. B. **(Overview Top View)**



1100	A4	2311	A5	2707	C4	3221	B4	3909	B4
1101	A3	2403	A1	2708	C4	3222	B4	4102	A3
1200	A4	2411	A2	2709	C4	3223	B4	4103	B3
1500	C2	2412	B1	2710	C4	3224	A3	4104	A3
1600	A1	2413	B1	2711	C4	3225	A3	4105	B3
1601	A1	2417	A2	2712	B4	3226	B4	4108	B2
1602	C1	2418	A2	2713	B4	3227	A5	4109	B2
1603	C2	2419	B2	2714	B4	3228	A4	4110	B2
1800	B1	2420	A1	2715	B3	3233	B4	4501	C1
1900	A2	2421	A1	2716	B4	3234	A4	4600	C1
1901	A1	2422	A1	2717	B4	3235	A4	4601	C1
2100	B2	2423	A1	2719	B4	3236	A5	4602	C1
2101	B3	2424	B1	2720	C4	3237	A5	4700	C5
2102	B3	2425	A2	2723	C4	3242	B4	4701	C5
2103	B3	2426	B2	2724	C5	3243	B4	5100	A2
2109	A3	2427	A2	2725	C4	3244	A5	5101	A3
2110	A3	2428	A2	2726	C4	3245	A5	5102	A4
2111	A3	2429	A2	2727	C4	3400	A1	5103	B3
2112	A3	2430	A1	2800	C3	3401	A1	5200	A4
2113	A3	2431	A1	2817	C4	3403	A1	5201	A5
2114	A3	2432	A2	2821	B1	3408	B1	5202	A5
2116	A2	2433	A2	2824	C3	3409	B1	5203	A4
2117	A2	2434	A2	2829	B1	3410	B1	5205	A4
2118	A2	2437	A2	2834	B1	3500	C1	5206	B5
2119	A2	2438	A2	2837	C3	3501	C1	5209	A4
2127	A3	2439	A1	2903	A2	3601	A5	5210	A4
2129	B3	2440	A1	2904	A2	3602	A5	5212	A4
2130	B2	2441	A2	2907	B3	3603	A5	5300	B4
2131	B2	2442	A2	2908	B2	3604	B1	5302	B4
2132	A4	2444	A1	2909	A2	3605	B1	5400	A2
2134	A4	2512	C1	2912	A1	3609	B1	5402	A1
2135	B3	2513	C1	2914	B3	3610	B2	5403	A2
2136	A3	2514	C1	3100	B3	3611	A5	5404	A2
2138	A3	2515	C2	3101	B3	3612	A5	5500	B1
2139	B3	2516	C1	3102	B3	3613	A5	5501	B1
2140	A3	2517	B1	3103	B2	3614	B2	5502	B1
2141	A3	2518	B1	3104	A4	3615	A1	5503	B2
2142	A3	2519	B2	3105	A4	3619	A1	5504	C1
2143	A3	2520	B1	3106	A3	3620	C2	5505	C1
2144	A3	2530	C2	3107	A2	3621	A5	5506	C1
2145	A3	2539	C1	3108	A3	3622	A5	5507	C1
2146	A2	2540	C1	3109	A3	3623	C1	5508	B2
2147	A4	2541	C1	3110	A3	3624	A5	5509	C2
2148	A4	2542	B2	3117	A3	3625	C1	5600	A5
2149	A4	2545	C2	3118	B1	3629	B1	5602	A5
2150	A4	2600	A5	3119	B2	3630	A1	5603	A5
2151	A4	2601	A5	3120	B3	3631	B2	5606	A1
2152	A3	2602	A5	3121	B3	3632	B1	5607	A1
2153	B2	2603	C1	3122	B3	3633	A1	5700	C4
2154	B2	2604	C1	3123	B3	3634	B2	5701	C4
2200	A4	2608	B1	3124	B3	3635	C1	5702	B3
2201	A4	2609	B1	3125	B2	3636	A1	5809	C4
2203	A4	2610	A5	3126	B3	3637	C1	5810	B3
2204	B4	2611	A5	3127	A3	3638	A1	5903	B3
2205	A4	2612	A5	3128	A3	3700	B4	5904	A1
2206	A5	2613	B1	3129	A3	3701	B3	5907	B3
2207	B4	2614	B2	3130	B3	3702	B3	7100	A3
2208	A4	2618	B1	3131	A4	3704	C4	7102	B3
2209	A5	2619	B2	3132	A4	3707	B4	7103	A4
2210	A4	2620	A5	3133	A4	3708	B4	7200	A4
2211	A5	2621	A5	3134	A4	3709	C4	7203	A4
2212	A5	2622	A5	3135	A4	3711	C4	7204	B5
2213	A4	2623	C1	3136	A3	3712	C4	7403	A2
2215	A4	2624	C1	3137	B2	3713	C5	7404	A2
2216	B4	2628	A1	3138	B2	3714	B4	7500	C2
2217	B4	2629	B1	3200	A4	3715	B5	7501	C1
2218	B5	2630	A1	3202	A3	3716	B5	7503	C2
2219	B5	2631	C1	3203	A5	3717	B5	7600	A5
2220	A5	2632	A1	3204	A4	3718	B4	7602	A1
2221	A5	2633	B2	3208	A3	3719	B4	7603	A5
2222	A4	2634	A1	3209	B5	3801	C3	7605	A5
2223	A4	2635	B2	3211	A4	3807	C3	7700	B4
2225	A4	2636	A5	3213	B4	3808	C3	7703	C5
2226	B4	2700	B4	3214	B4	3812	C3	7802	C3
2227	B4	2701	B4	3215	A4	3816	C3	7803	C3
2228	A5	2702	B4	3216	B4	3818	C3		
2230	A4	2703	C4	3217	B4	3819	C3		
2231	A3	2704	C4	3218	B4	3824	C3		
2304	B4	2705	C4	3219	A4	3825	C3		
2305	B4	2706	C4	3220	A4	3907	A3		

■ PRINTED CIRCUIT BOARD

DIGITAL P. C. B. **(Part 1 Top View)**

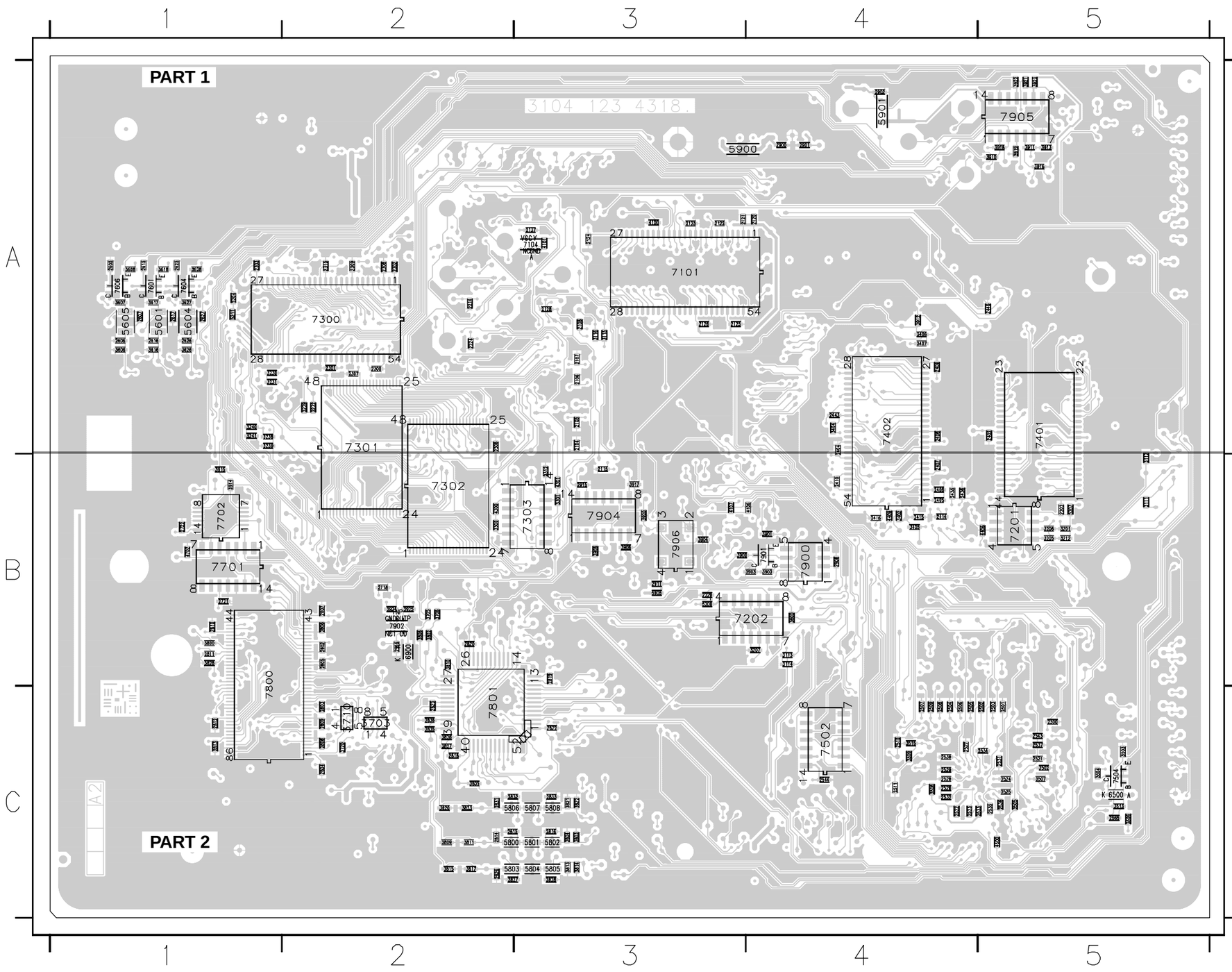


■ PRINTED CIRCUIT BOARD

DIGITAL P. C. B. **(Part 2 Top View)**

■ PRINTED CIRCUIT BOARD

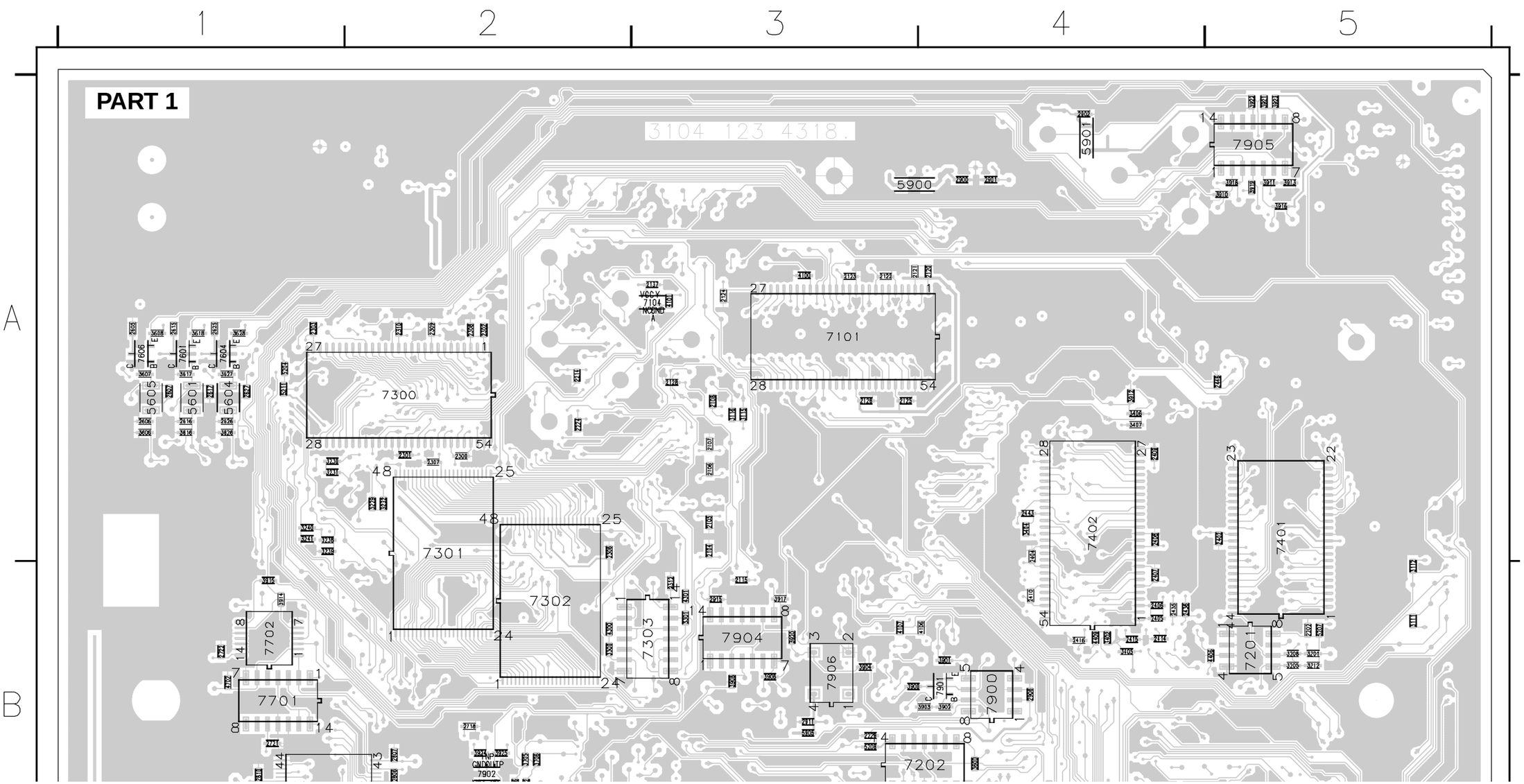
DIGITAL P. C. B. **(Overview Bottom View)**



2104	A3	2802	B2	3803	C3	7702	B1
2105	A3	2803	C2	3804	C3	7800	B1
2106	A3	2804	C2	3805	C2	7801	C2
2107	A3	2805	B2	3806	B2	7900	B4
2108	A3	2806	B2	3809	C2	7901	B4
2115	B3	2807	B2	3810	B2	7902	B2
2120	A4	2808	C2	3811	C2	7904	B3
2121	A3	2809	C2	3813	C3	7905	A5
2122	A3	2810	B1	3814	C3	7906	B3
2123	A3	2811	B1	3815	C2		
2124	A3	2812	C1	3817	C2		
2125	A3	2813	C1	3820	C2		
2126	A3	2814	C2	3821	C3		
2128	A3	2815	C2	3822	C3		
2137	A3	2816	C3	3823	C2		
2202	B5	2818	C2	3826	C2		
2214	A2	2819	B3	3827	C2		
2224	A2	2820	B2	3828	B1		
2229	B3	2822	C3	3900	B3		
2300	A2	2823	C2	3901	B4		
2301	A2	2826	C2	3902	B4		
2302	A2	2827	C2	3903	B4		
2303	A1	2828	C3	3904	B3		
2306	A2	2831	C2	3906	B3		
2307	A2	2832	C2	3908	B3		
2308	A2	2833	C3	3910	A5		
2309	A2	2835	C2	3911	A5		
2310	A2	2836	C2	3912	A4		
2312	B3	2900	A4	3913	A5		
2402	A5	2901	A4	3914	B1		
2404	A4	2902	A4	3915	B1		
2405	B4	2906	B4	3916	A5		
2406	B4	2911	B3	3917	B3		
2407	B4	2915	B3	3918	A5		
2408	A4	2916	B2	3919	A5		
2409	A4	3111	B5	3920	B3		
2410	B4	3112	B5	3921	A5		
2414	B4	3113	B4	3922	A5		
2415	B4	3114	B4	3923	A5		
2416	B4	3115	A3	3924	B2		
2435	B4	3116	A3	3925	B2		
2436	B4	3201	B5	4100	A3		
2443	A4	3205	B5	4101	A3		
2446	A5	3206	B5	4106	B4		
2500	C5	3207	B4	4107	B3		
2501	C5	3212	B5	4300	B2		
2502	C5	3229	A2	4301	B3		
2503	C5	3230	A1	4406	B5		
2504	C4	3231	A1	4409	B4		
2505	C4	3232	A2	4500	C5		
2506	C4	3238	A1	4702	B1		
2507	C4	3239	A1	5204	A1		
2508	C4	3240	A1	5207	B5		
2509	C4	3241	A1	5208	B3		
2510	C4	3300	B2	5211	A1		
2511	C4	3301	B3	5601	A1		
2521	C5	3402	B4	5604	A1		
2522	C4	3404	A4	5605	A1		
2523	C4	3405	B4	5800	C2		
2524	C5	3406	A4	5801	C3		
2525	C5	3407	A4	5802	C3		
2526	C4	3502	C5	5803	C2		
2527	C4	3503	C5	5804	C3		
2528	C4	3504	C5	5805	C3		
2529	C4	3505	C5	5806	C2		
2531	C5	3506	C5	5807	C3		
2532	C4	3507	C5	5808	C3		
2533	C5	3508	C4	5900	A3		
2534	C5	3509	C4	5901	A4		
2535	C5	3513	C5	5905	B3		
2536	C5	3515	C4	6500	C5		
2537	C5	3600	B4	6900	B2		
2538	C4	3606	A1	7101	A3		
2543	C5	3607	A1	7104	A3		
2544	C4	3608	A1	7201	B5		
2565	C5	3616	A1	7202	B4		
2605	A1	3617	A1	7300	A2		
2606	A1	3618	A1	7301	A2		
2607	A1	3626	A1	7302	B2		
2615	A1	3627	A1	7303	B3		
2616	A1	3628	A1	7401	A5		
2617	A1	3703	C2	7402	A4		
2625	A1	3705	B2	7502	C4		
2626	A1	3706	B2	7504	C5		
2627	A1	3710	C2	7601	A1		
2718	B2	3720	C2	7604	A1		
2721	B1	3800	B1	7606	A1		
2722	B1	3802	B2	7701	B1		

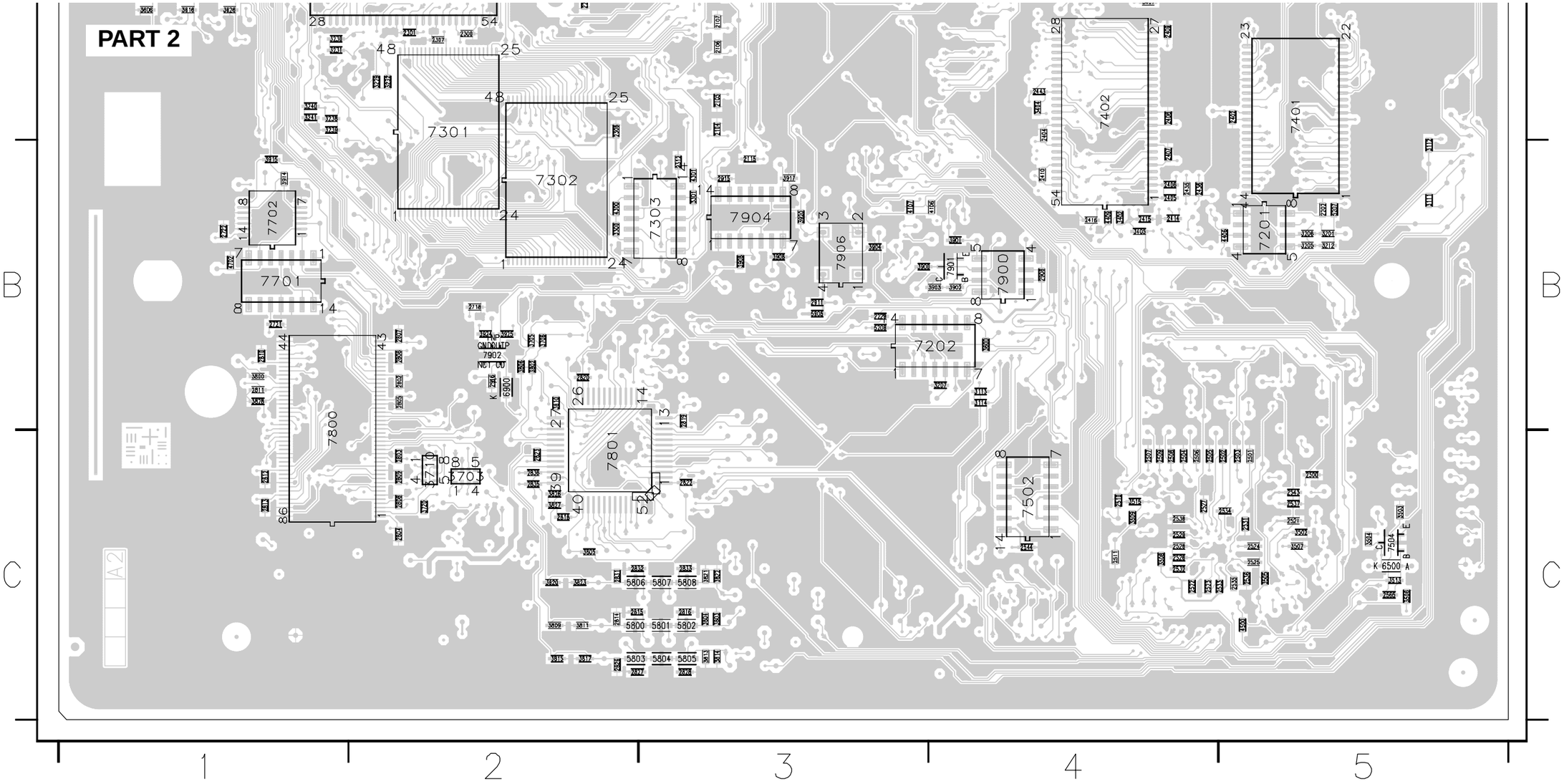
■ PRINTED CIRCUIT BOARD

DIGITAL P. C. B. **(Part 1 Bottom View)**



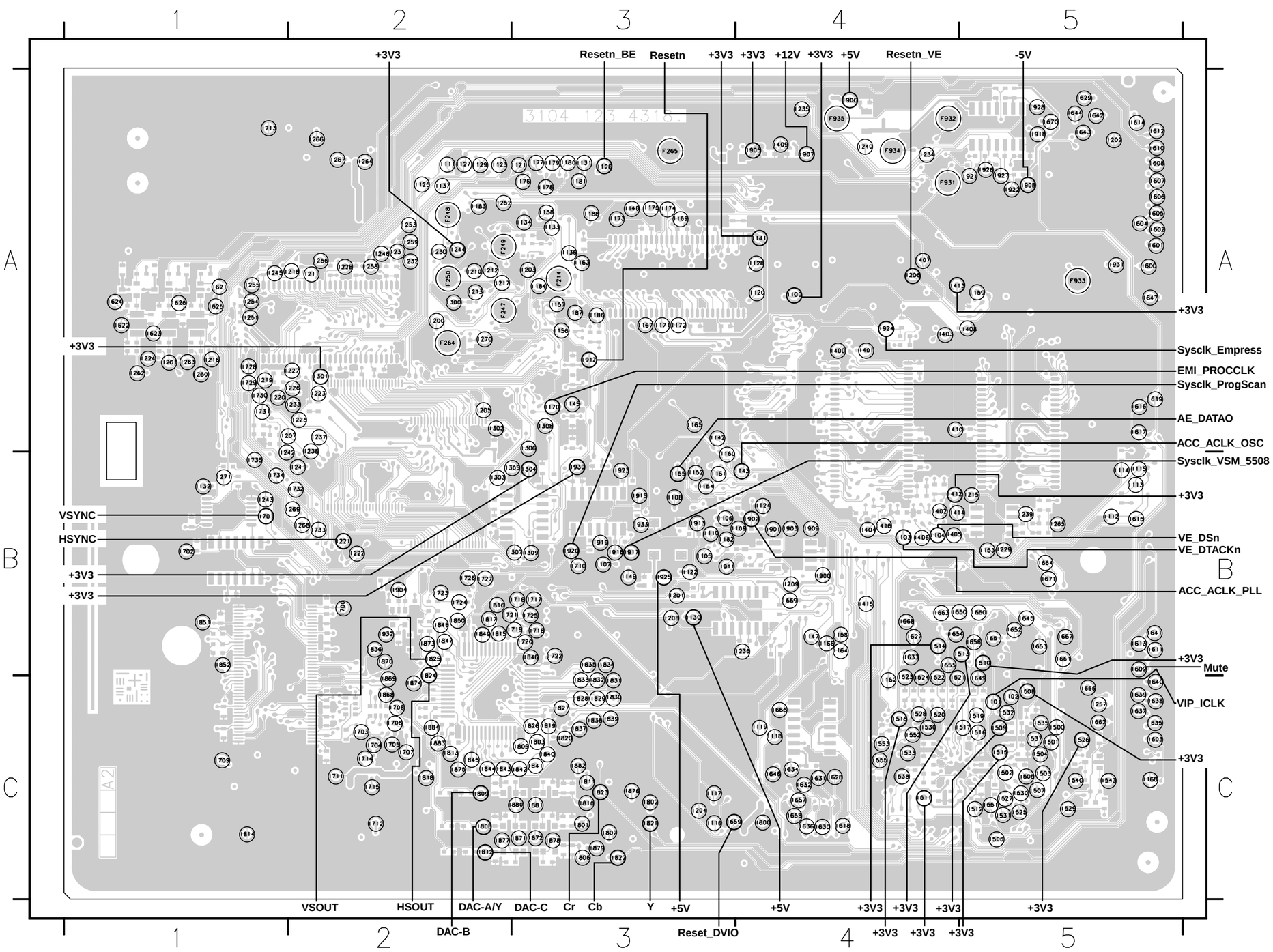
■ PRINTED CIRCUIT BOARD

DIGITAL P. C. B. **(Part 2 Bottom View)**



■ PRINTED CIRCUIT BOARD

DIGITAL P. C. B. (Testlands Bottom View)



■ PRINTED CIRCUIT BOARD

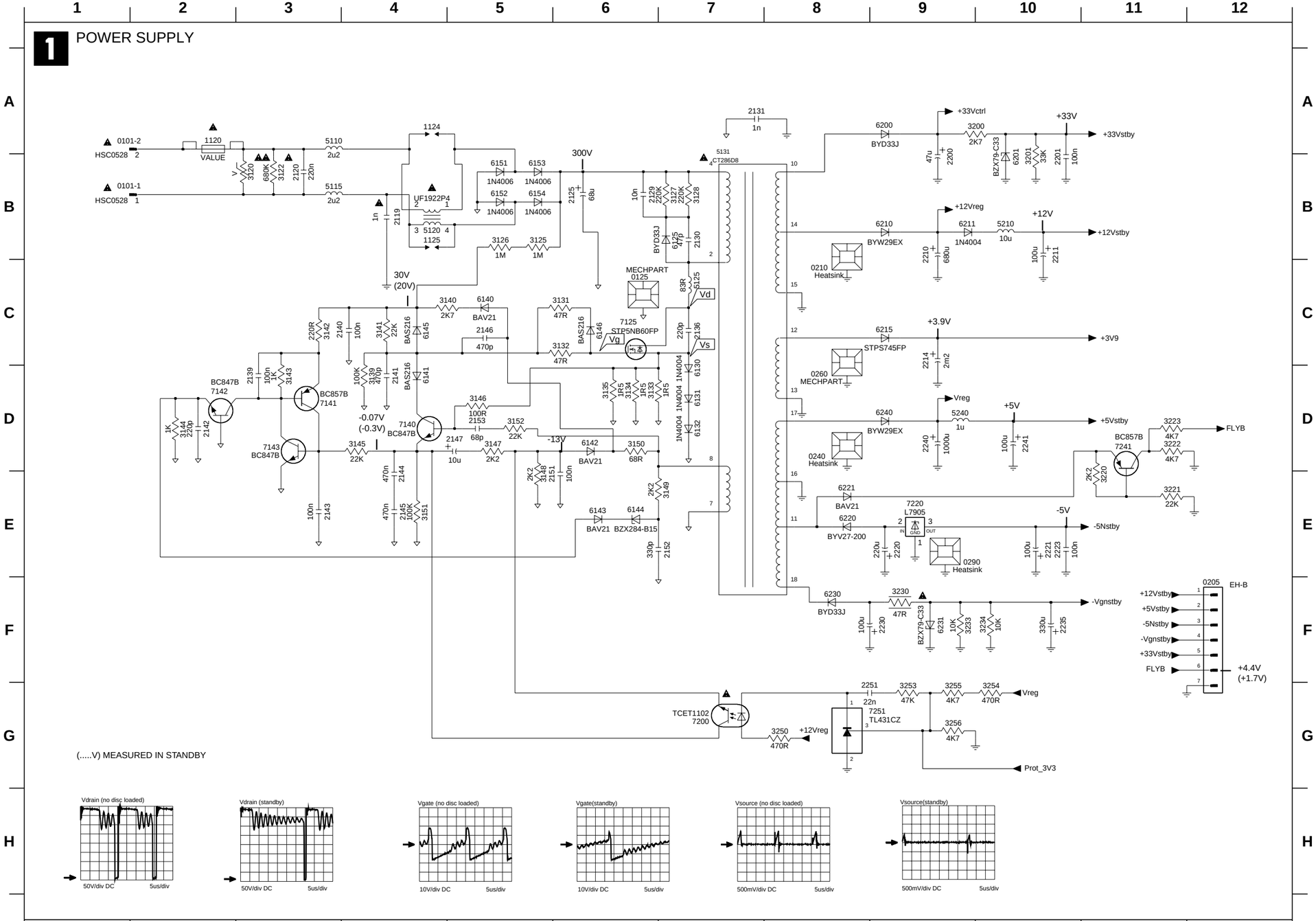
DIGITAL P. C. B. (Mapping Testlands)

F214	A3	I175	A3	I300	A2	I610	A5	I720	B3	I880	C3
F247	A2	I176	A3	I301	A2	I611	B5	I721	B2	I881	C3
F248	A2	I177	A3	I302	A2	I612	A5	I722	B3	I882	C3
F249	A2	I178	A3	I303	B2	I613	B5	I723	B2	I883	C2
F250	A2	I179	A3	I304	B3	I614	A5	I724	B2	I884	C2
F264	A2	I180	A3	I305	B3	I615	B5	I725	B3	I900	B4
F265	A3	I181	A3	I306	A3	I616	A5	I726	B2	I901	B4
F931	A4	I182	B3	I307	B3	I617	A5	I727	B2	I902	B4
F932	A4	I183	A2	I308	A3	I618	C4	I728	A1	I903	B4
F933	A5	I184	A3	I309	B3	I619	A5	I729	A1	I904	B2
F934	A4	I186	A3	I400	A4	I621	A1	I730	A1	I905	A4
F935	A4	I187	A3	I401	A4	I622	A1	I731	A1	I906	A4
I100	A4	I188	A3	I402	B4	I623	A1	I732	B2	I907	A4
I101	C5	I200	A2	I403	A4	I624	A1	I733	B2	I908	A5
I102	C5	I201	B3	I404	B4	I625	A1	I734	B1	I909	B4
I103	B4	I202	A5	I405	B4	I626	A1	I735	B1	I911	B3
I104	B4	I203	A3	I406	B4	I627	B4	I800	C4	I912	A3
I105	B3	I204	C3	I407	A4	I628	C4	I801	C3	I913	B3
I106	B3	I205	A2	I408	A5	I629	A5	I802	C3	I915	B3
I107	B3	I206	A4	I409	A4	I630	C4	I803	C3	I916	B3
I108	B3	I207	A2	I410	A4	I631	C4	I805	C3	I917	B3
I109	B4	I208	B3	I412	B4	I632	C4	I806	C3	I918	A5
I110	B3	I209	B4	I413	A4	I633	B4	I807	C3	I919	B3
I111	A2	I210	A2	I414	B4	I634	C4	I808	C2	I920	B3
I112	B5	I211	A2	I415	B4	I635	C5	I809	C2	I921	A5
I113	B5	I212	A2	I416	B4	I636	C4	I810	C3	I922	A5
I114	B5	I213	A2	I500	C5	I637	C5	I811	C3	I923	B3
I115	B5	I215	B5	I501	C5	I638	C5	I812	C2	I924	A4
I116	C3	I216	A1	I502	C5	I639	C5	I813	C2	I925	B3
I117	C3	I217	A2	I503	C5	I640	C5	I814	C1	I926	A5
I118	C4	I218	A2	I504	C5	I641	B5	I815	B2	I927	A5
I119	C4	I219	A1	I505	C5	I642	A5	I816	B2	I928	A5
I120	A4	I220	A1	I506	C5	I643	A5	I817	B2	I930	B3
I121	A3	I221	B2	I507	C5	I644	A5	I818	C2	I931	A5
I122	B3	I222	B2	I508	C5	I645	B5	I819	C3	I932	B2
I123	A2	I223	A2	I509	C5	I646	C4	I820	C3	I933	B3
I124	B4	I224	A1	I510	B5	I647	A5	I821	C3
I125	A2	I225	A2	I511	C4	I649	C5	I822	C3
I126	A3	I226	A2	I512	C5	I650	B4	I823	C3
I127	A2	I227	A2	I513	B5	I651	B5	I824	B2
I128	A4	I228	A2	I514	B4	I652	B5	I825	B2
I129	A2	I229	B5	I515	C5	I653	B5	I826	C3
I130	B3	I230	A2	I516	C5	I654	B4	I827	C3
I131	A3	I231	A2	I517	C5	I655	B4	I828	C3
I132	B1	I232	A2	I518	C4	I656	B5	I829	C3
I133	A3	I233	A2	I519	C5	I657	C4	I830	C3
I134	A3	I234	A4	I520	C4	I658	C4	I831	C3
I136	A3	I235	A4	I521	C4	I659	C3	I832	C3
I137	A2	I236	B4	I522	C4	I660	B5	I833	C3
I138	A3	I237	A2	I523	C4	I661	B5	I834	B3
I140	A3	I238	A2	I524	C4	I662	C5	I835	B3
I141	A4	I239	B5	I525	C5	I663	B4	I836	B2
I142	A3	I240	A4	I526	C5	I664	B5	I837	C3
I143	B4	I241	B2	I527	C5	I665	C4	I838	C3
I145	A3	I242	B1	I528	C4	I666	C5	I839	C3
I147	B4	I243	B1	I529	C5	I667	B5	I840	C3
I149	B3	I244	A2	I530	C5	I668	B4	I841	C3
I152	B3	I245	A1	I531	C5	I669	B4	I842	C3
I153	B5	I246	A2	I532	C5	I670	A5	I843	C2
I154	B3	I251	A1	I533	C4	I671	B5	I844	C2
I155	B3	I252	A2	I535	C5	I700	B2	I845	C2
I156	A3	I253	A2	I536	C4	I701	B1	I846	B3
I157	A3	I254	A1	I537	C5	I702	B1	I847	B2
I158	B4	I255	A1	I538	C4	I703	C2	I848	B2
I159	A5	I256	A2	I540	C5	I704	C2	I849	B2
I160	B3	I257	C5	I543	C5	I705	C2	I850	B2
I161	B3	I258	A2	I551	C5	I706	C2	I851	B1
I162	C4	I259	A2	I552	C4	I707	C2	I852	B1
I163	A3	I260	A1	I553	C4	I708	C2	I868	C2
I164	B4	I261	A1	I555	C4	I709	C1	I869	C2
I165	A3	I262	A1	I600	A5	I710	B3	I870	B2
I166	B4	I263	A1	I601	A5	I711	C2	I871	C3
I167	A3	I264	A2	I602	A5	I712	C2	I872	C3
I168	C5	I265	B5	I603	C5	I713	A1	I873	B2
I169	A3	I266	A2	I604	A5	I714	C2	I874	C2
I170	A3	I267	A2	I605	A5	I715	C2	I875	C2
I171	A3	I268	B2	I606	A5	I716	B3	I876	C3
I172	A3	I269	B2	I607	A5	I717	B3	I877	C2
I173	A3	I270	A2	I608	A5	I718	B3	I878	C3
I174	A3	I271	B1	I609	B5	I719	B3	I879	C3

■ SCHEMATIC DIAGRAM **A, B, G model**

POWER SUPPLY

1 POWER SUPPLY



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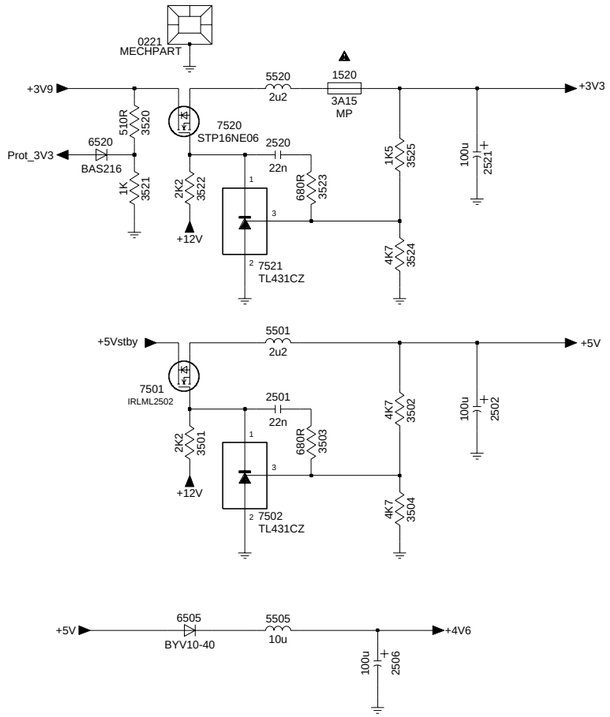
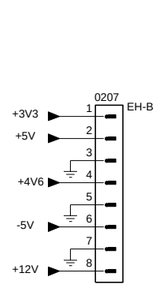
0101-2 A1
0125 C6
0205 F12
0210 C8
0240 D8
0260 D8
0290 E9
1120 A2
1124 A4
1125 B4
2119 B4
2120 B3
2125 B6
2126 B6
2127 A4
2129 B6
2130 B7
2131 A7
2136 C7
2139 D3
2140 C4
2141 D4
2142 D2
2143 E3
2144 E4
2145 E4
2146 C5
2147 D5
2151 E5
2152 E7
2153 D5
2200 B9
2201 B10
2210 B9
2211 B10
2212 B9
2214 C9
2215 C9
2220 E9
2221 E10
2222 E10
2223 E10
2230 F9
2235 F10
2240 D9
2241 D10
2242 D9
2251 G9
3120 B3
3122 B3
3123 B2
3125 B5
3126 B5
3127 B7
3128 B7
3129 A5
3131 C6
3132 C6
3133 D6
3134 D6
3135 D6
3139 D4
3140 C5
3141 C4
3142 C3
3143 D3
3144 D2
3145 D4
3146 D5
3147 D5
3148 E5
3149 E7
3150 D6
3151 E4
3152 D5
3200 A10
3201 B10
3220 E11
3221 E11
3222 D11
3223 D11
3230 F9
3233 F9
3234 F10
3250 G8
3253 G9
3254 G10
3255 G9
3256 G9
5110 A3
5115 B3
5120 B4
5121 B4
5125 C7
5131 B7
5210 B10
5240 D9
6125 B7
6128 A4
6129 A5
6130 D7
6131 D7
6132 D7
6140 C5
6141 D4
6142 D6
6143 E6
6144 E6
6145 C4
6146 C6
6151 B5
6152 B5
6153 B5
6154 B5
6200 A9
6201 B10
6210 B9
6211 B9
6215 C9
6220 E8
6221 E8
6230 F8
6231 F9
6240 D9
7125 C6
7140 D4
7141 D3
7142 D2
7143 D3
7200 G7
7220 E9
7241 D11
7251 G8
9110 A3
9115 B3

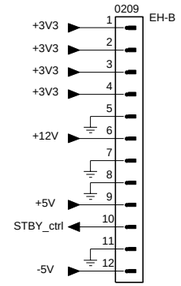
■ SCHEMATIC DIAGRAM **A, B, G model**

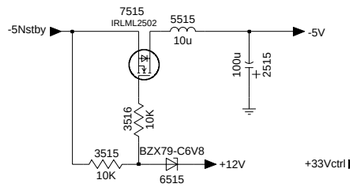
POWER SUPPLY

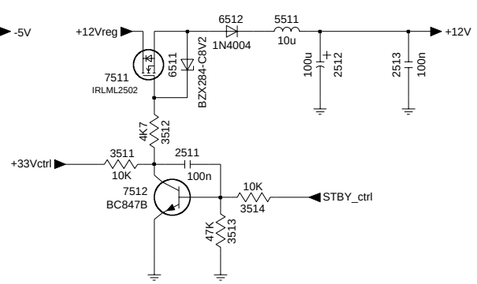
2 POWER SUPPLY

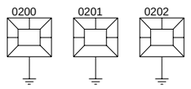












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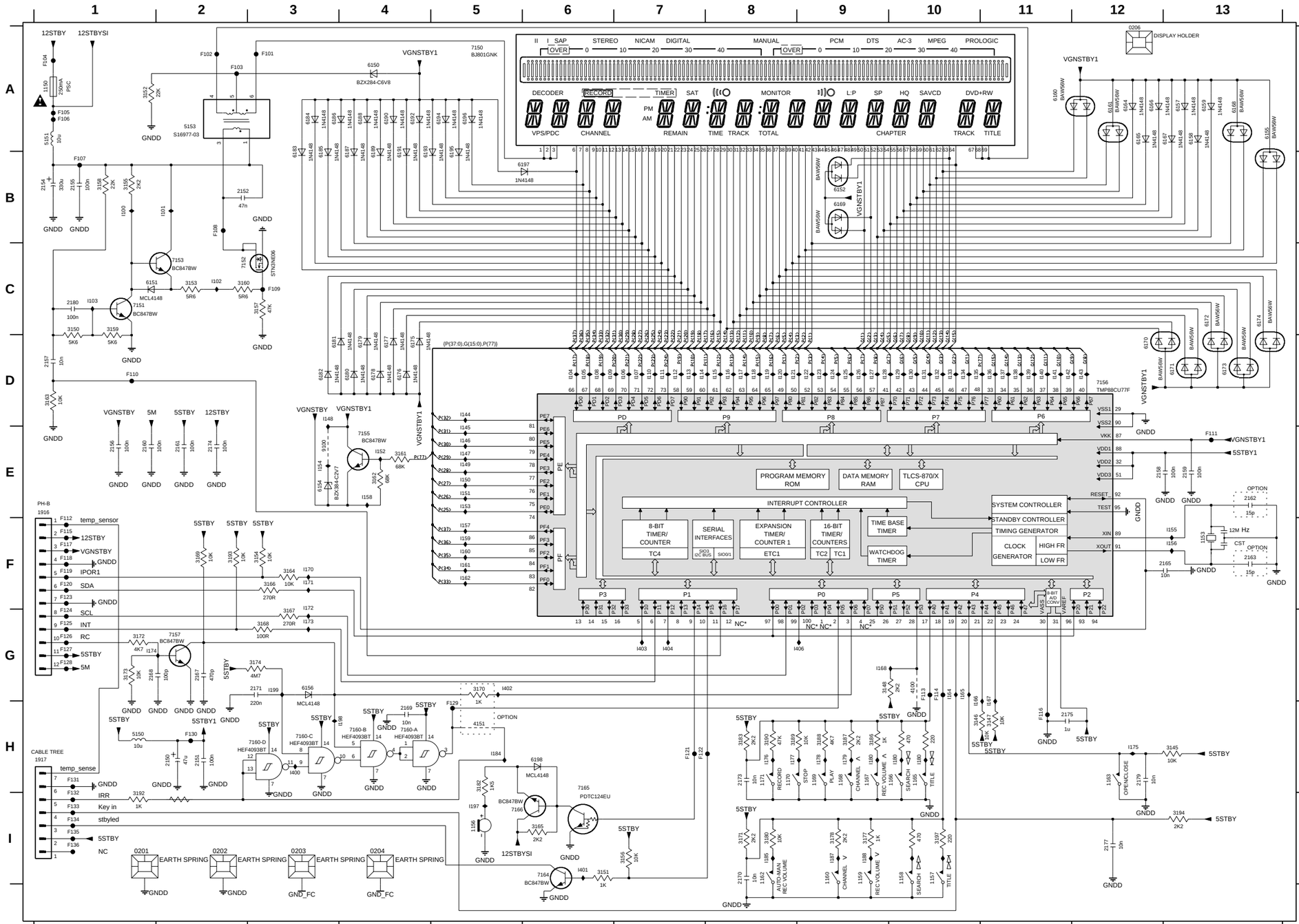
0202 G11
0207 B8
0209 A10
0221 B3
1520 B4
2501 D4
2502 D5
2506 F4
2511 E9
2512 E10
2513 E11
2515 E8
2520 B4
2521 B5
3501 D3
3502 D4
3503 D4
3504 E4
3511 E9
3512 E9
3513 F9
3514 E10
3515 E7
3516 E7
3520 B3
3521 C3
3522 C3
3523 C4
3524 C4
3525 B4
5501 C4
5505 E4
5511 D10
5515 D7
5520 B4
6505 E3
6511 E9
6512 D9
6515 E7
6520 B2
7501 D3
7502 E3
7511 E9
7512 E9
7515 D7
7520 B3
7521 C3

■ SCHEMATIC DIAGRAM

DISPLAY



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0203 I3	6179 D4	2156 E1	7156 D12
0204 I4	6180 D4	2157 D1	7157 G2
0206 A12	6181 D3	2158 E12	7160-A H4
1150 A1	6182 D3	2159 E13	7160-B H4
1153 F13	6183 B3	2160 E1	7160-C H3
1156 I5	6184 A3	2161 E2	7160-D H3
1159 I9	6185 B3	2162 E13	7164 I6
1160 I9	6186 A3	2163 F13	7165 H6
1162 I8	6187 B4	2165 F13	7166 I6
1163 H12	6188 A4	2167 G2	9100 E3
1167 H9	6189 B4	2168 G1	F101 A3
1168 H9	6190 A4	2169 H4	F102 A2
1169 H9	6191 B4	2170 I8	F103 A2
1170 H8	6192 A4	2171 G3	F104 A1
1171 H8	6193 B4	2173 H8	F105 A1
1174 I10	6194 A5	2174 E2	F106 A1
1916 E1	6195 B5	2175 H11	F107 B1
1917 H1	6196 A5	2177 I12	F108 B2
2150 H2	6197 B6	2179 H12	F109 C3
2151 H2	6198 H6	2180 C1	F110 D1
2152 B2	7150 A5	3145 H13	F111 E13
2154 B1	7151 C1	3146 H10	F112 F1
2155 B1	7152 C2	3147 H11	F113 G10
2156 E1	7153 C2	3148 G9	F114 G10
2157 D1	7155 E4	3150 C1	F115 F1
2158 E12	7156 D12	3151 I6	F116 H11
2159 E13	7157 G2	3152 A1	F117 F1
2160 E1	7160-A H4	3153 C2	F118 F1
2161 E2	7160-B H4	3154 F3	F119 F1
2162 E13	7160-C H3	3155 B1	F120 F1
2163 F13	7160-D H3	3156 I7	F121 H7
2165 F13	7164 I6	3157 C3	F122 H7
2167 G2	7165 H6	3158 B1	F123 F1
2168 G1	7166 I6	3159 C1	F124 G1
2169 H4	9100 E3	3160 C2	F125 G1
2170 I8	F101 A3	3161 E4	F126 G1
2171 G3	F102 A2	3162 E4	F127 G1
2173 H8	F103 A2	3163 D1	F128 G1
2174 E2	F104 A1	3164 F3	F129 H5
2175 H11	F105 A1	3165 I6	F130 H2
2177 I12	F106 A1	3166 F3	F131 H1
2179 H12	F107 B1	3167 G3	F132 I1
2180 C1	F108 B2	3168 G3	F133 I1
3145 H13	F109 C3	3169 F2	F134 I1
3146 H10	F110 D1	3170 G5	F135 I1
3147 H11	F111 E13	3171 I8	F136 I1
3148 G9	F112 F1	3172 G1	
3150 C1	F113 G10	3173 G1	
3151 I6	F114 G10	3174 G3	
3152 A1	F115 F1	3177 I9	
3153 C2	F116 H11	3178 I9	
3154 F3	F117 F1	3180 I8	
3155 B1	F118 F1	3182 H5	
3156 I7	F119 F1	3183 H8	
3157 C3	F120 F1	3186 H9	
3158 B1	F121 H7	3187 H9	
3159 C1	F122 H7	3188 H9	
3160 C2	F123 F1	3189 H8	
3161 E4	F124 G1	3190 H8	
3162 E4	F125 G1	3192 I1	
3163 D1	F126 G1	3193 F2	
3164 F3	F127 G1	3194 I13	
3165 I6	F128 G1	3197 I10	
3166 F3	F129 H5	4100 G10	
3167 G3	F130 H2	4151 H5	
3168 G3	F131 H1	5150 H1	
3169 F2	F132 I1	5151 A1	
3170 G5	F133 I1	5153 A2	
3171 I8	F134 I1	6150 A4	
3172 G1	F135 I1	6151 C1	
3173 G1	F136 I1	6152 B9	
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3177 I9		6155 A13	
3178 I9		6156 G3	
3180 I8		6157 A13	
3182 H5		6158 A13	
3183 H8		6159 A13	
3186 H9		6160 A11	
3187 H9		6161 A12	
3188 H9		6164 A12	
3189 H8		6165 A12	
3190 H8		6166 A12	
3192 I1		6167 A13	
3193 F2		6168 A13	
3194 I13		6169 B9	
3197 I10		6170 D12	
4100 G10		6171 D13	
4151 H5		6172 C13	
5150 H1		6173 D13	
5151 A1		6174 C13	
5153 A2		6175 D4	
6150 A4		6176 D4	
6151 C1			
6152 B9			
6154 E3			
6155 A13			
6156 G3			
6157 A13			
6158 A13			
6159 A13			
6160 A11			
6161 A12			
6164 A12			
6165 A12			
6166 A12			
6167 A13			
6168 A13			
6169 B9			
6170 D12			
6171 D13			
6172 C13			
6173 D13			
6174 C13			
6175 D4			
6176 D4			

■ SCHEMATIC DIAGRAM

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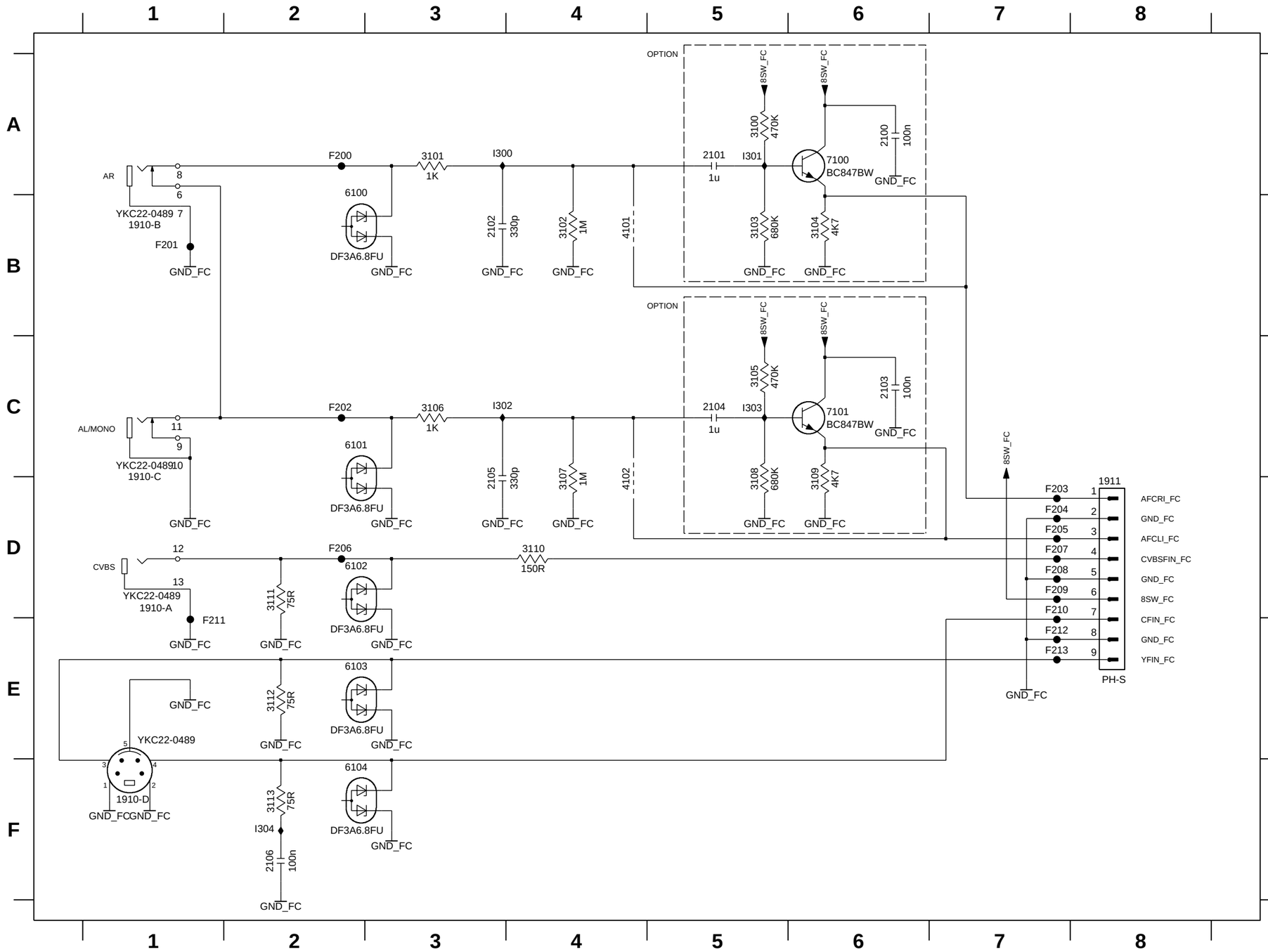

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1910-C C1
1910-D F1
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2100 A6
2101 A5
2102 B3
2103 C6
2104 C5
2105 D3
2106 F2
3100 A5
3101 A3
3102 B4
3103 B5
3104 B6
3105 C5
3106 C3
3107 D4
3108 D5
3109 D6
3110 D4
3111 D2
3112 E2
3113 F2
4101 B4
4102 D4
6100 A3
6101 C3
6102 D3
6103 E3
6104 F3
7100 A6
7101 C6
F200 A2
F201 B1
F202 C2
F203 D7
F204 D7
F205 D7
F206 D2
F207 D7
F208 D7
F209 D7
F210 D7
F211 E1
F212 E7
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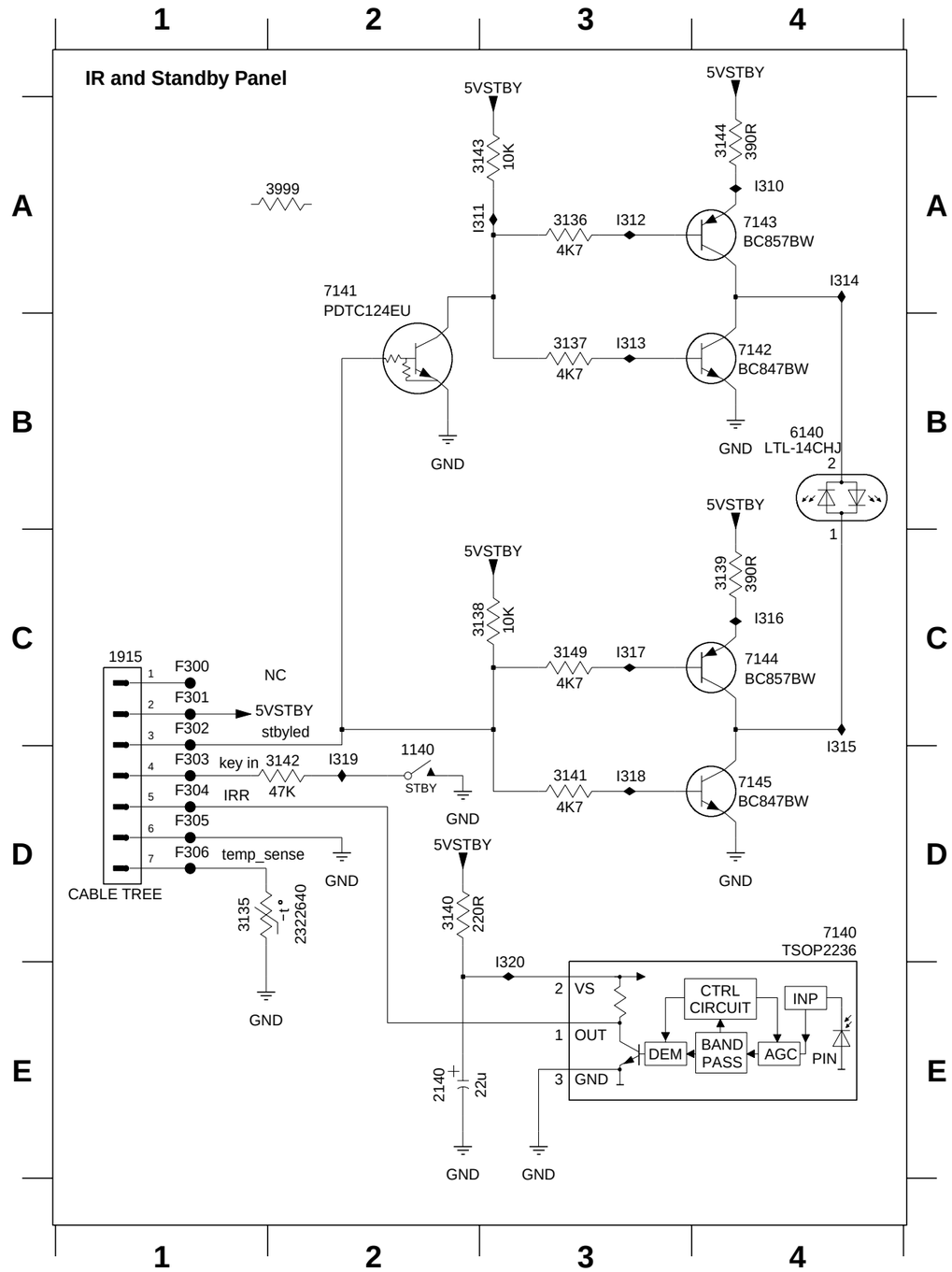
I300 A3
I301 A5
I302 C3
I303 C5
I304 F2

■ SCHEMATIC DIAGRAM

IR AND STANDBY



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3138 C3
3139 C4
3140 D2
3141 D3
3142 D2
3143 A3
3144 A4
3149 C3
3999 A2
6140 B4
7140 D4
7141 A2
7142 B4
7143 A4
7144 C4
7145 D4
F300 C1
F301 C1
F302 C1
F303 D1
F304 D1
F305 D1
F306 D1
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I316 C4
I317 C3
I318 D3
I319 D2
I320 D3

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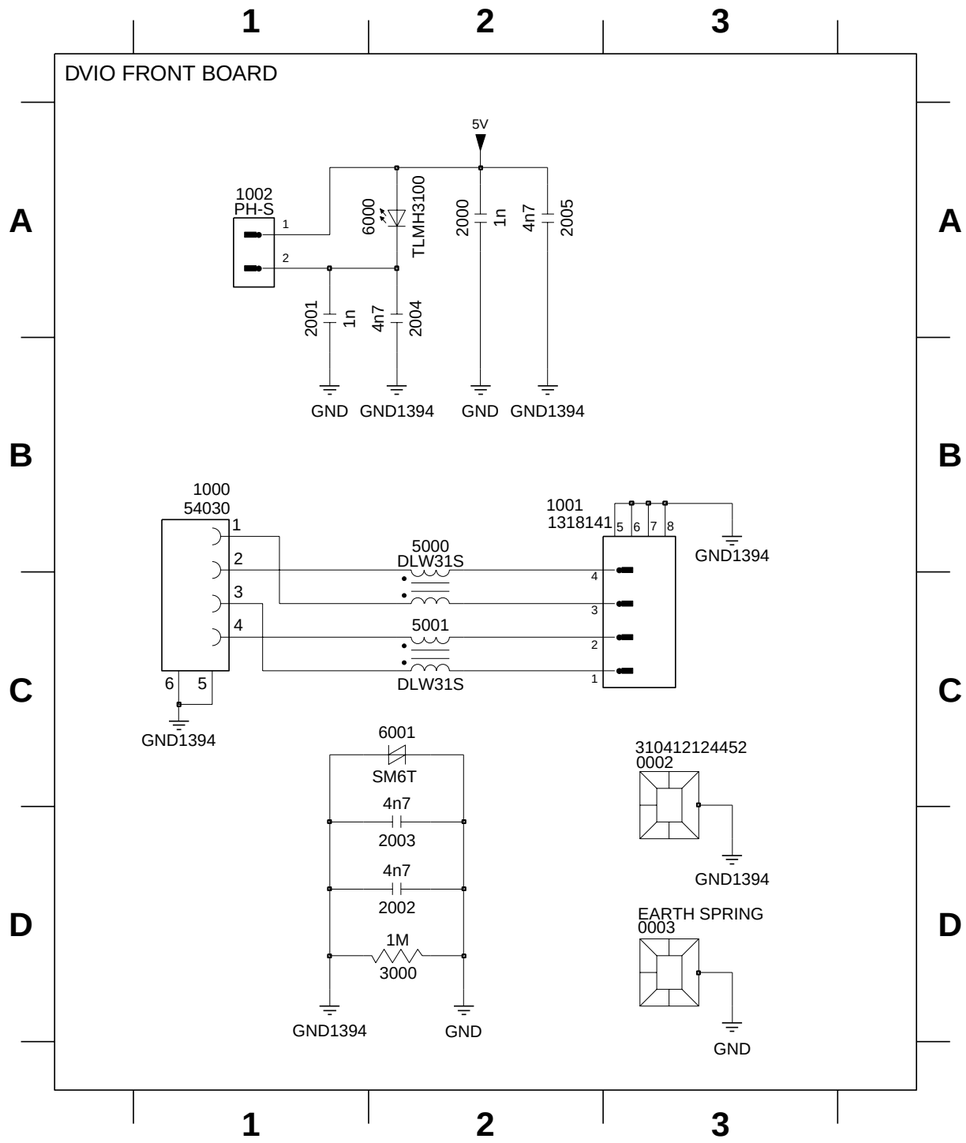
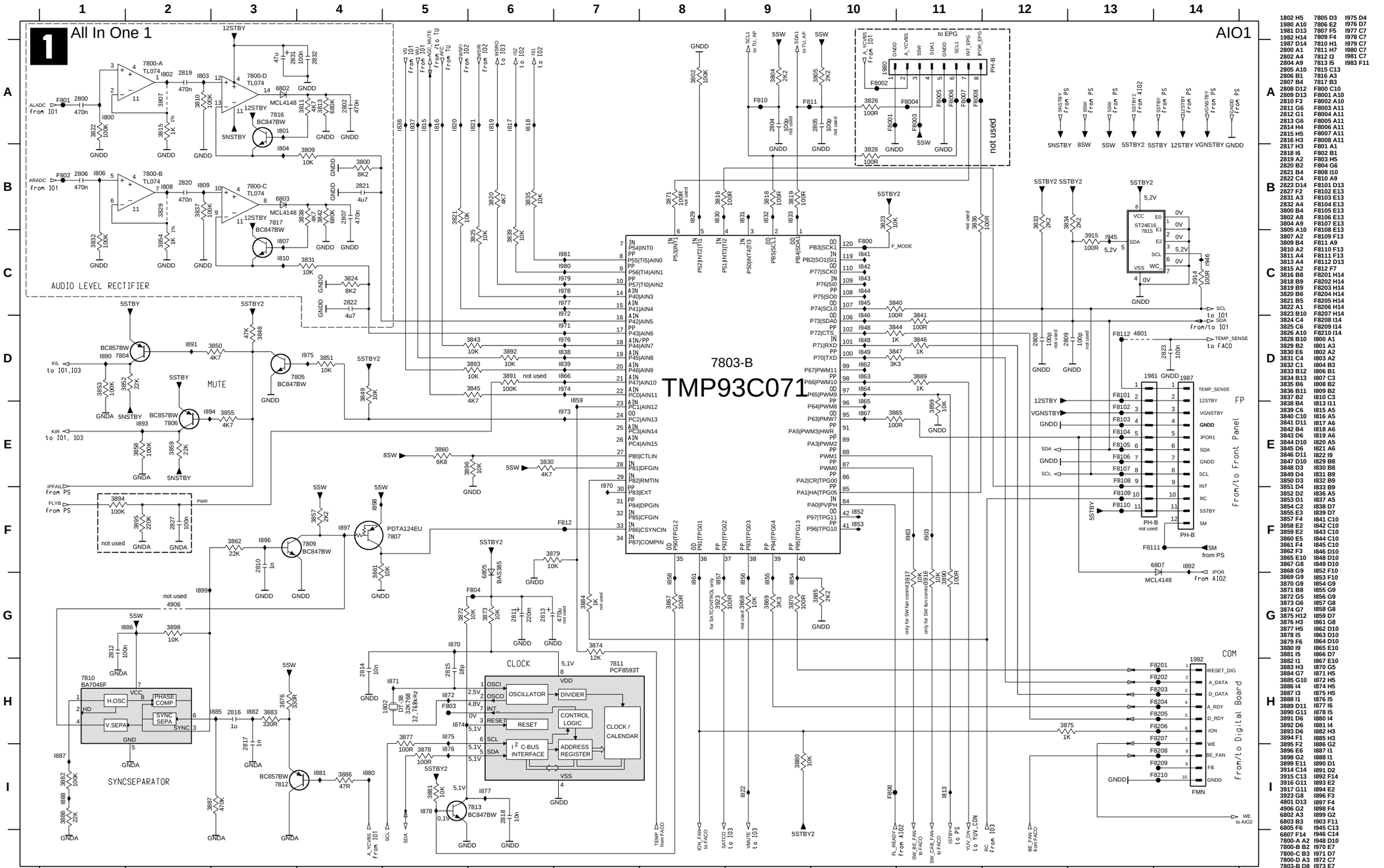


■ SCHEMATIC DIAGRAM **U model**

ANALOG: All in One 1



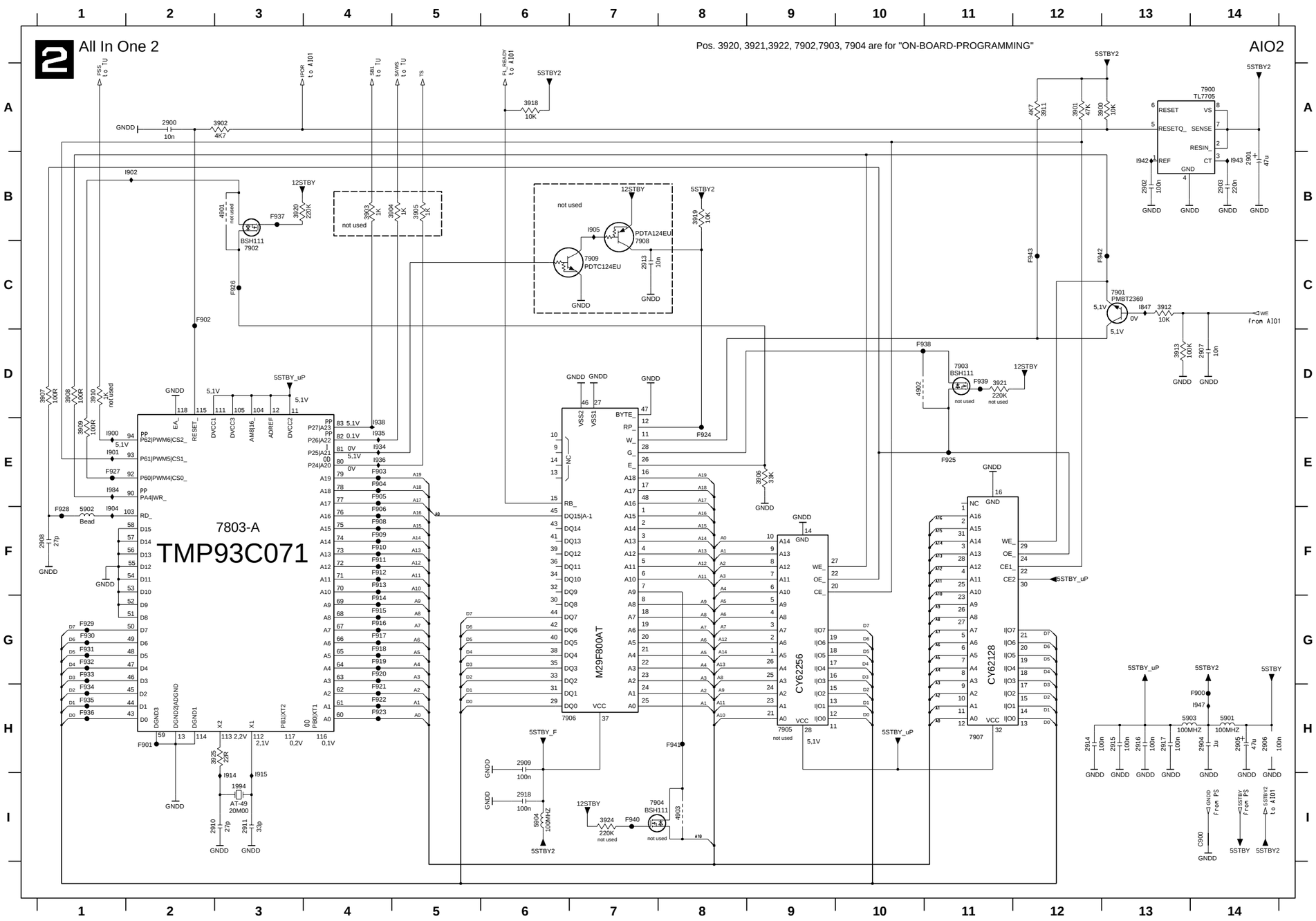
1802 H5 1980 A10 1981 D13 1982 H14 1987 D14 2800 A1 2802 A4 2804 A9 2805 A10 2806 B1 2807 B4 2808 D12 2809 D13 2810 F3 2811 G6 2812 G1 2813 G6 2814 H4 2815 H5 2816 H3 2817 H3 2818 I6 2819 A2 2820 B2 2821 B4 2822 C4 2823 D14 2827 F2 2831 A3 2832 A4 3800 B4 3802 A8 3804 A9 3805 A10 3807 A2 3809 B4 3810 A2 3811 A4 3813 A4 3815 A2 3816 B8 3818 B9 3819 B9 3820 B6 3821 B5 3822 A1 3823 B10 3824 C4 3825 C6 3826 A10 3828 B10 3829 B2 3830 E6 3831 C4 3832 C1 3833 B12 3834 B13 3835 B6 3836 B11 3837 B2 3838 B4 3839 C6 3840 C10 3841 D11 3842 B4 3843 D6 3844 D10 3845 D6 3846 D11 3847 D10 3848 D3 3849 D4 3850 D3 3851 D4 3852 D2 3853 D1 3854 C2 3855 E3 3857 F4 3858 E2 3859 E2 3860 E5 3861 F4 3862 F3 3865 E10 3867 G8 3868 G9 3869 G9 3870 G9 3871 B8 3872 G5 3873 G6 3874 G7 3875 H12 3876 H3 3877 H5 3878 I5 3879 F6 3880 I9 3881 I5 3882 I1 3883 H3 3884 G7 3885 G10 3886 I4 3887 I3 3888 I1 3889 D11 3890 G11 3891 D6 3892 D6 3893 D6 3894 F1 3895 F2 3896 E6 3898 G2 3899 E11 3914 C14 3915 C13 3916 G11 3917 G11 3923 G8 4801 D13 4906 G2 6802 A3 6803 B3 6805 F6 6807 F14 7800-A A2 7800-B B2 7800-C B3 7800-D A3 7803-B D8 7804 D2

7805 D3 7806 E2 7807 F5 7809 F4 7810 H1 7811 H7 7812 I3 7813 I5 7815 C13 7816 A3 7817 B3 F800 C10 F8001 A10 F8002 A10 F8003 A11 F8004 A11 F8005 A11 F8006 A11 F8007 A11 F8008 A11 F801 A1 F802 B1 F803 H5 F804 G6 F808 I10 F810 A9 F8101 D13 F8102 E13 F8103 E13 F8104 E13 F8105 E13 F8106 E13 F8107 E13 F8108 E13 F8109 E13 F8110 E13 F8111 E13 F8112 4801 F8201 H14 F8202 H14 F8203 H14 F8204 H14 F8205 H14 F8206 H14 F8207 H14 F8208 I14 F8209 I14 F8210 I14 I800 A1 I801 A3 I802 A2 I803 A2 I804 B3 I806 B1 I807 C3 I808 B2 I809 B2 I810 D1 I811 I1 I815 A5 I816 A5 I817 A6 I818 A6 I819 A6 I820 A5 I821 A6 I822 I9 I829 B8 I830 B8 I831 B9 I832 B9 I833 B9 I836 A5 I837 A5 I838 D7 I839 D7 I841 C10 I842 C10 I843 C10 I844 C10 I845 C10 I846 D10 I848 D10 I849 D10 I852 F10 I853 F10 I854 G9 I855 G9 I856 G9 I857 G8 I858 G8 I859 D7 I861 G8 I862 D10 I863 D10 I864 D10 I865 E10 I866 D7 I867 E10 I870 G5 I871 H5 I872 H5 I874 H5 I875 H5 I876 I5 I877 I6 I878 I5 I880 I4 I881 I4 I882 H3 I885 H3 I886 G2 I887 I1 I890 D1 I891 D2 I892 F14 I893 E2 I894 E2 I896 F3 I897 F4 I898 B8 I899 G2 I903 F11 I945 C13 I946 C14 I948 D10 I970 E7 I971 D7 I973 E7 I974 D7

■ SCHEMATIC DIAGRAM

U model

ANALOG: All in One 2



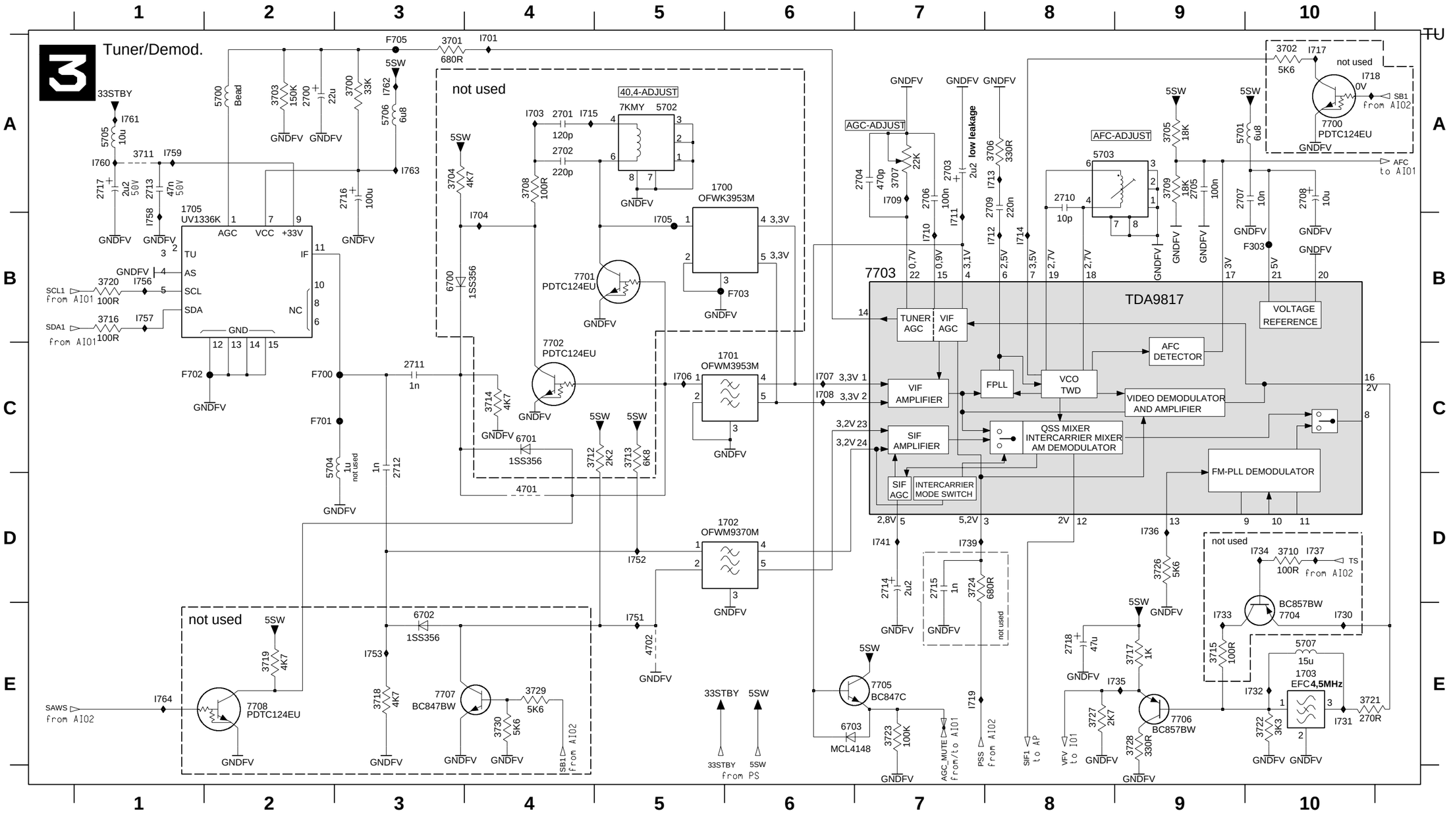
1994 I3
2900 A2
2901 B14
2902 B13
2903 B14
2904 H14
2905 H14
2906 H14
2907 D14
2908 F1
2909 H6
2910 I3
2911 I3
2913 C7
2914 H12
2915 H13
2916 H13
2917 H13
2918 I6
3900 A13
3901 A12
3902 A3
3903 B4
3904 B5
3905 B5
3906 E9
3907 D1
3908 D1
3909 E1
3910 D1
3911 A12
3912 C13
3913 D13
3918 A6
3919 B8
3920 B3
3921 D11
3924 I7
3925 H3
4901 B3
4902 D10
4903 I8
5901 H14
5902 F1
5903 H13
5904 I6
7803-A F3
7900 A14
7901 C13
7902 C3
7903 D11
7904 I7
7905 H9
7906 H7
7907 H11
7908 B7
7909 C7
C900 I14
F900 H14
F901 H2
F902 C2
F903 E4
F904 E4
F905 E4
F906 F4
F908 F4
F909 F4
F910 F4
F911 F4
F912 F4
F913 F4
F914 G4
F915 G4
F916 G4
F917 G4
F918 G4
F919 G4
F920 G4
F921 H4
F922 H4
F923 H4
F924 E8
F925 E11
F926 C3
F927 E1
F928 F1
F929 G1
F930 G1
F931 G1
F932 G1
F933 G1
F934 H1
F935 H1
F936 H1
F937 B3
F938 D10
F939 D11
F940 I7
F941 H8
F942 C13
F943 C12
I847 C13
I900 E1
I901 E1
I902 B2
I904 F1
I905 B7
I914 I3
I915 I3
I934 E4
I935 E4
I936 E4
I938 E4
I942 B13
I943 B14
I947 H14
I984 E1

■ SCHEMATIC DIAGRAM

U model

ANALOG: TUBER / DEMODULATOR

1700 A5	2700 A2	2705 A9	2710 A8	2715 D7	3701 A3	3706 A8	3711 A1	3716 B1	3721 E10	3727 E8	4702 E5	5704 C2	6701 C4	7702 C4	7707 E3	F702 C1	I704 B4	I709 A7	I714 B8	I730 E10	I735 E9	I751 E5	I758 B1	I763 A3
1701 C5	2701 A4	2706 A7	2711 C3	2716 A3	3702 A10	3707 A7	3712 C4	3717 E9	3722 E10	3728 E9	5700 A2	5705 A1	6702 E3	7703 B7	7708 E2	F703 B6	I705 B5	I710 B7	I715 A4	I731 E10	I736 D9	I752 D5	I759 A1	I764 E1
1702 D5	2702 A4	2707 A9	2712 C3	2717 A1	3703 A2	3708 A4	3713 C5	3718 E3	3723 E7	3729 E4	5701 A9	5706 A3	6703 E6	7704 E10	F303 B10	F705 A3	I706 C5	I711 B7	I717 A10	I732 E10	I737 D10	I753 E3	I760 A1	
1703 E10	2703 A7	2708 A10	2713 A1	2718 E8	3704 A3	3709 A9	3714 C4	3719 E2	3724 D7	4701 D4	5702 A5	5707 E10	7700 A10	7705 E7	F700 C2	I701 A4	I707 C6	I712 B8	I718 A10	I733 E9	I739 D7	I756 B1	I761 A1	
1705 A1	2704 A7	2709 A8	2714 D7	3700 A3	3705 A9	3710 D10	3715 E9	3720 B1	3726 D9		5703 A8	6700 B3	7701 B5	7706 E9	F701 C2	I703 A4	I708 C6	I713 A8	I719 E7	I734 D10	I741 D7	I757 B1	I762 A3	

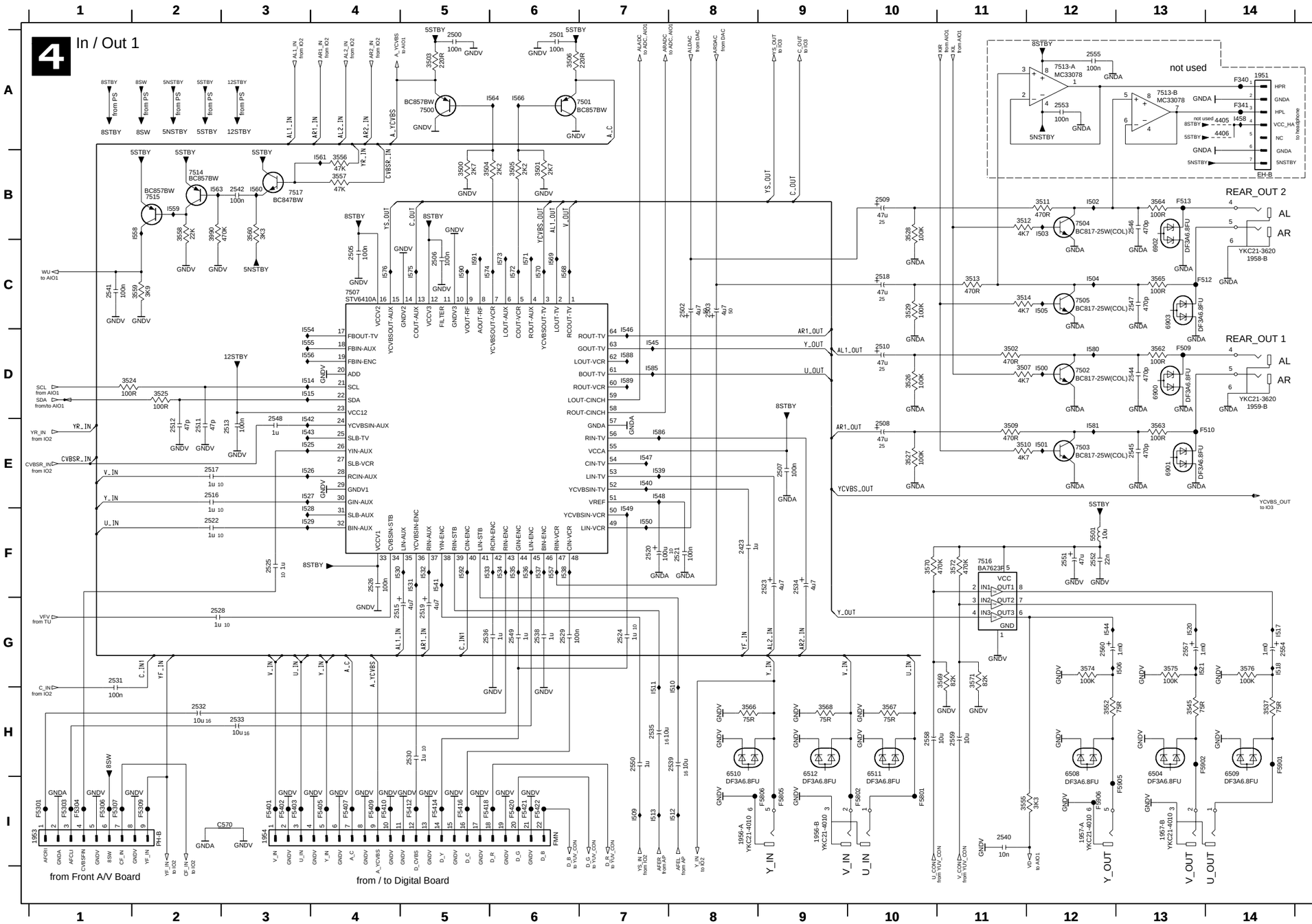


■ SCHEMATIC DIAGRAM

U model

ANALOG: IN / OUT 1

4 In / Out 1



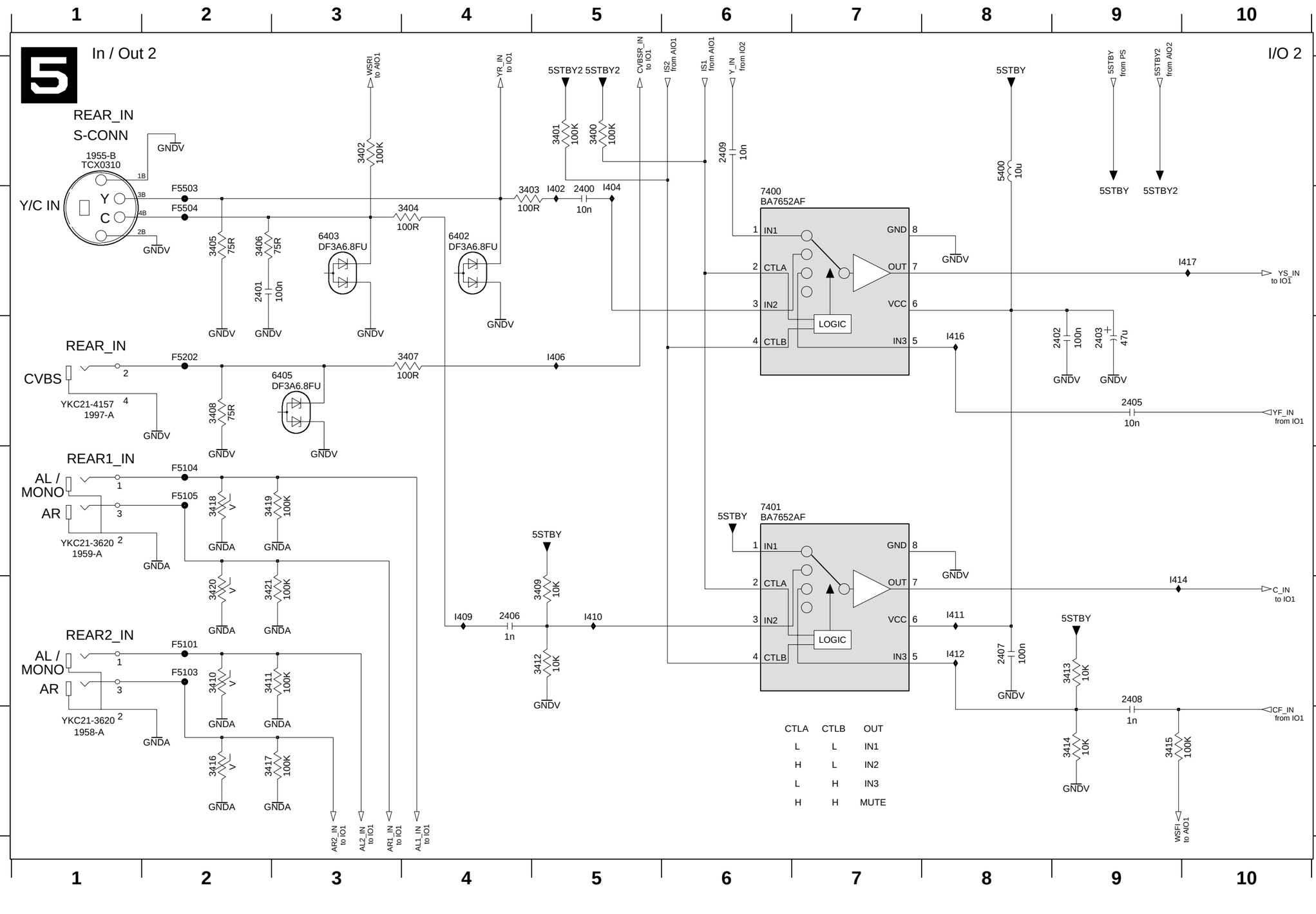
I/O

1951 A14	6512 H9	I576 C4	
1953 I1	6900 D13	I580 D12	
1954 I3	6901 E13	I581 E12	
1956-A I8	6902 B13	I585 D7	
1956-B I9	6903 C13	I586 E7	
1957-A I12	7500 A5	I588 D7	
1957-B I13	7501 A6	I589 D7	
1958-B C14	7502 D12	I590 C5	
1959-B D14	7503 E12	I591 C5	
2423 F8	7504 B12	I592 F5	
2500 A5	7505 C12		
2501 A6	7507 C4		
2502 C8	7513-A A12		
2503 C8	7513-B A13		
2505 C4	7514 B2		
2506 C5	7515 B2		
2507 E9	7516 F11		
2508 E10	7517 B3		
2509 B10	C570 I3		
2510 D10	F340 A14		
2511 E2	F341 A14		
2512 E2	F509 D13		
2513 E3	F510 E14		
2515 G4	F512 C13		
2516 E2	F513 B13		
2517 E2	F5301 I1		
2518 C10	F5303 I1		
2519 G5	F5304 I1		
2520 F7	F5306 I1		
2521 F8	F5307 I1		
2522 E2	F5309 I2		
2523 F9	F5401 I3		
2524 G7	F5402 I3		
2525 F3	F5403 I3		
2526 F4	F5405 I4		
2528 G2	F5407 I4		
2529 G6	F5409 I4		
2530 H5	F5410 I4		
2531 C1	F5412 I5		
2532 H2	F5414 I5		
2533 H3	F5416 I5		
2534 F9	F5418 I5		
2535 H7	F5420 I6		
2536 G5	F5421 I6		
2538 G6	F5422 I6		
2539 H8	F5801 I10		
2540 I11	F5802 I10		
2541 C1	F5805 I9		
2542 B3	F5806 I9		
2544 D13	F5901 H14		
2545 E13	F5902 H13		
2546 B13	F5905 I13		
2547 C13	F5906 I12		
2548 E3	I458 A14		
2549 G6	I500 D12		
2550 H7	I501 E12		
2551 F12	I502 B12		
2552 F12	I503 B12		
2553 A12	I504 C12		
2554 G14	I505 C12		
2555 A12	I506 G13		
2557 G13	I509 I7		
2558 H10	I510 G8		
2559 H11	I511 H7		
2560 G12	I512 I8		
3500 B5	I513 I7		
3501 B6	I514 D3		
3502 D11	I515 D3		
3503 A5	I517 G14		
3504 B5	I518 G14		
3505 B6	I520 G13		
3506 A6	I521 G13		
3507 D11	I525 E3		
3509 E11	I526 E3		
3510 E11	I527 E3		
3511 B12	I528 F3		
3512 B11	I529 F3		
3513 C11	I530 F4		
3514 C11	I531 F5		
3524 D1	I532 F5		
3525 D2	I533 F5		
3526 D10	I534 F6		
3527 E10	I535 F6		
3528 B10	I536 F6		
3529 C10	I537 F6		
3537 H14	I538 F6		
3545 H13	I539 E7		
3552 H12	I540 E7		
3555 I11	I541 F5		
3556 B4	I542 E3		
3557 B4	I543 E3		
3558 B2	I544 G12		
3559 C2	I545 D7		
3560 B3	I546 D7		
3562 D13	I547 E7		
3563 E13	I548 E7		
3564 B13	I549 F7		
3565 C13	I550 F7		
3566 H8	I554 D3		
3567 H10	I555 D3		
3568 H9	I556 D3		
3569 G11	I557 F6		
3570 F10	I558 B2		
3571 G11	I559 B2		
3572 F11	I560 B3		
3574 C12	I561 B4		
3575 G13	I563 B2		
3576 G14	I564 A6		
3990 B2	I566 A6		
4405 A14	I568 C6		
4406 A14	I569 C6		
5501 F12	I570 C6		
6504 H13	I571 C6		
6508 H12	I572 C6		
6509 H14	I573 C6		
6510 H8	I574 C5		
6511 H10	I575 C5		

■ SCHEMATIC DIAGRAM

U model

ANALOG: IN / OUT 2

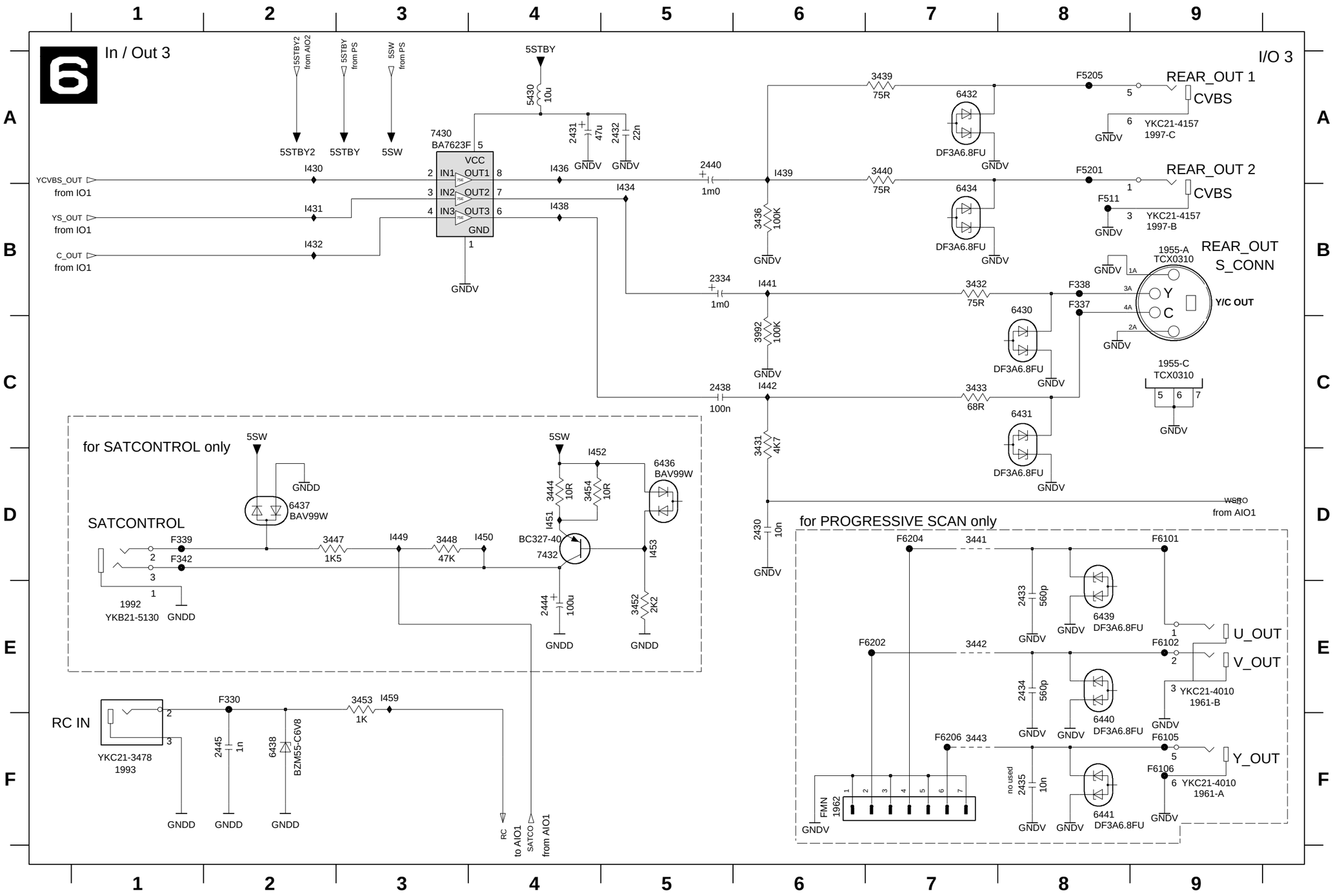


1952-A C1
1955-B A1
1958-A F1
1959-A D1
2400 B5
2401 B2
2402 C9
2403 C9
2405 C9
2406 E4
2407 E8
2408 E9
2409 A6
3400 A5
3401 A5
3402 A3
3403 B4
3404 B4
3405 B2
3406 B2
3407 C4
3408 C2
3409 E5
3410 E2
3411 E2
3412 E5
3413 E9
3414 F9
3415 F9
3416 F2
3417 F2
3418 D2
3419 D2
3420 E2
3421 E2
5400 A8
6402 B4
6403 B3
6405 C3
7400 B6
7401 D6
F5101 E2
F5103 E2
F5104 D2
F5105 D2
F5202 C2
F5503 A2
F5504 B2
I402 B5
I404 B5
I406 C5
I409 E4
I410 E5
I411 E8
I412 E8
I414 E9
I416 C8
I417 B10

■ SCHEMATIC DIAGRAM

U model

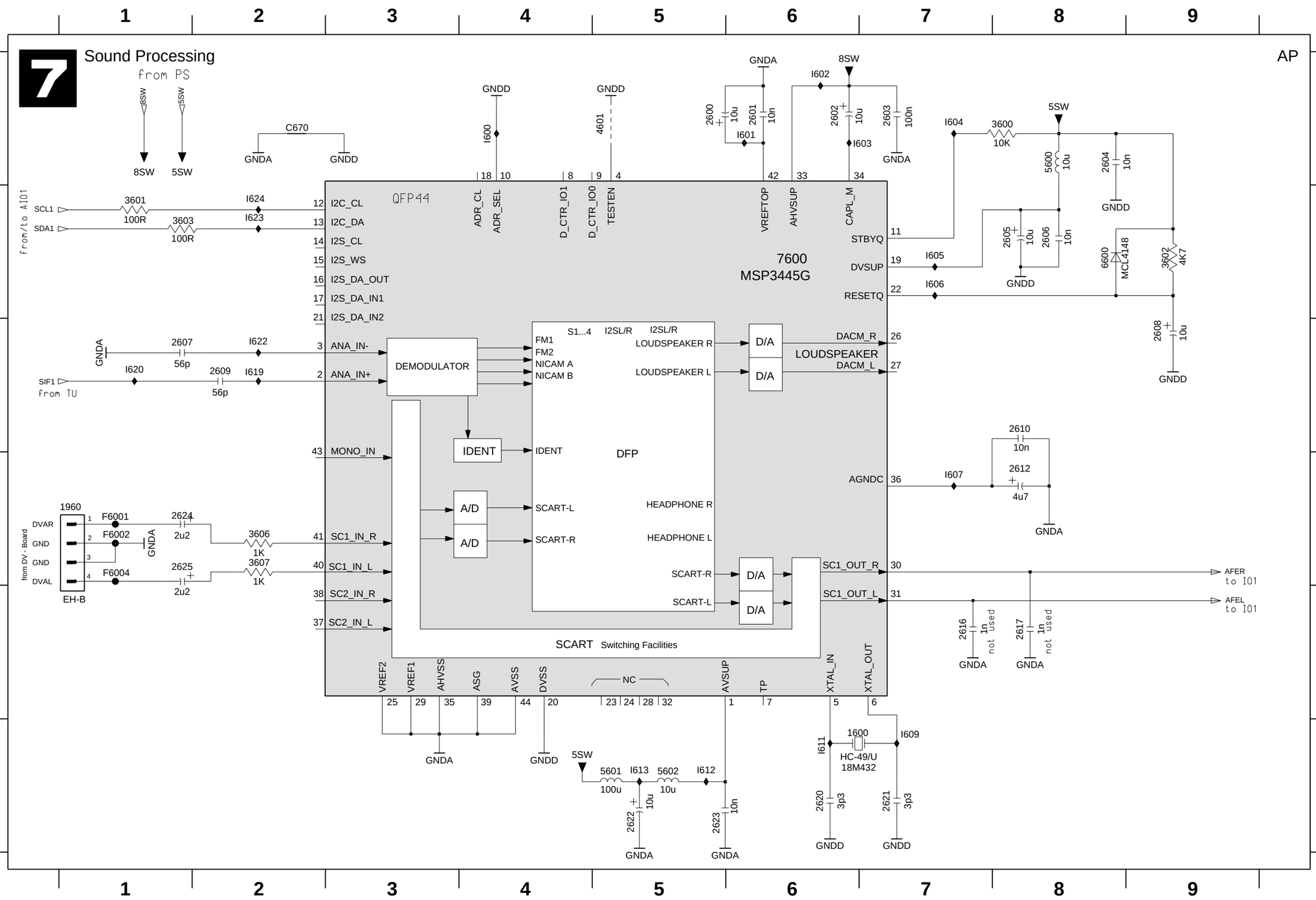
ANALOG: IN / OUT 3



1955-A B9
1955-C C9
1961-A F9
1961-B E9
1962 F6
1992 E1
1993 F1
1997-B B9
1997-C A9
2334 B5
2430 D6
2431 A4
2432 A5
2433 E8
2434 E8
2435 F8
2438 C5
2440 A5
2444 E4
2445 F2
3431 C6
3432 B7
3433 C7
3436 B6
3439 A7
3440 A7
3441 D7
3442 E7
3443 F7
3444 D4
3447 D2
3448 D3
3452 E5
3453 E3
3454 D4
3992 C6
5430 A4
6430 B8
6431 C8
6432 A7
6434 B7
6436 D5
6437 D2
6438 F2
6439 E8
6440 F8
6441 F8
7430 A3
7432 D4
F330 E2
F337 B8
F338 B8
F339 D1
F342 D1
F511 B8
F5201 A8
F5205 A8
F6101 D9
F6102 E9
F6105 F9
F6106 F9
F6202 E7
F6204 D7
F6206 F7
I430 A2
I431 B2
I432 B2
I434 B5
I436 A4
I438 B4
I439 A6
I441 B6
I442 C6
I449 D3
I450 D4
I451 D4
I452 D4
I453 D5
I459 E3

■ SCHEMATIC DIAGRAM **U model**

ANALOG: SOUND PROCESSING

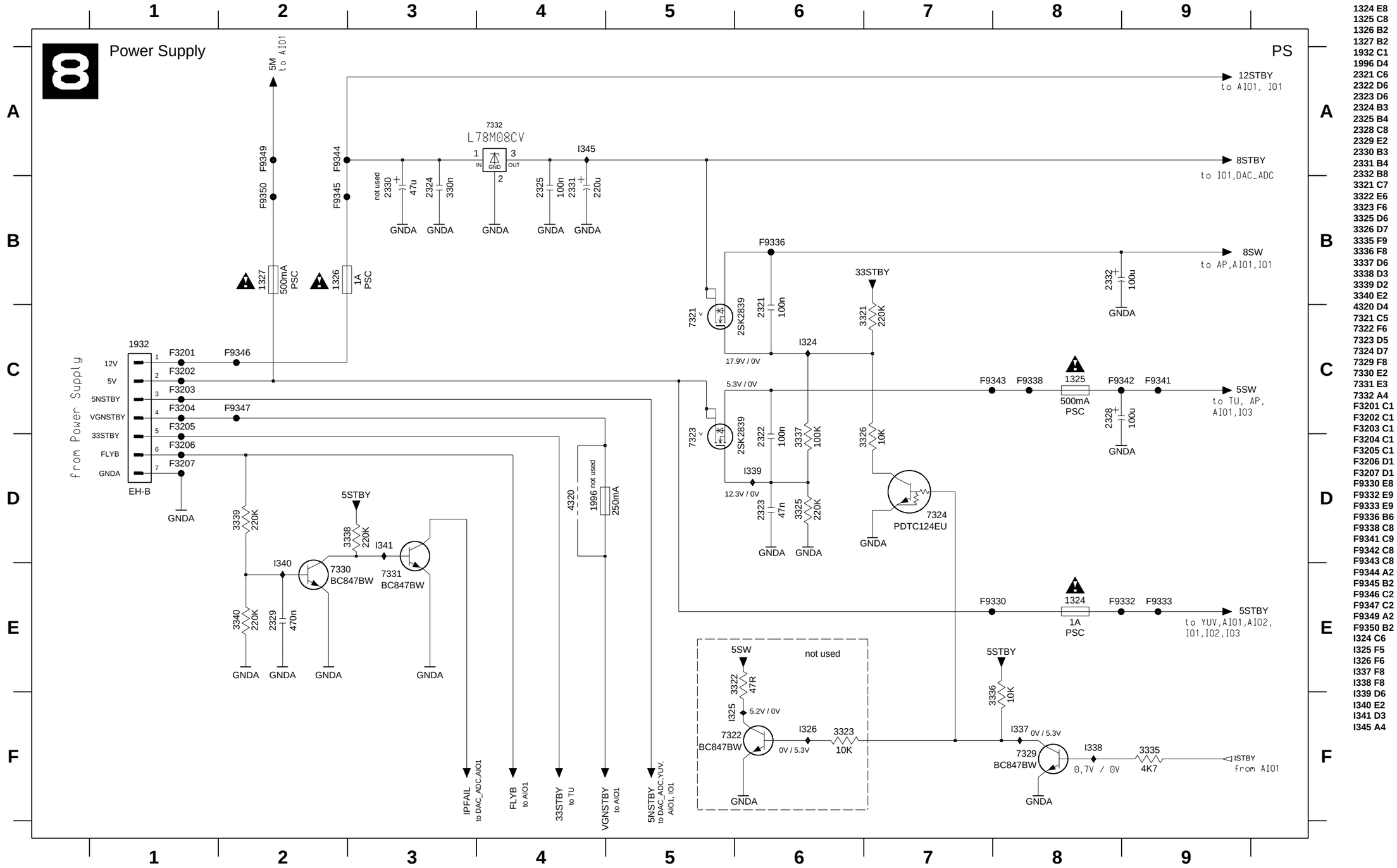


1600 F6
1960 D1
2600 A5
2601 A6
2602 A6
2603 A7
2604 A8
2605 B8
2606 B8
2607 C1
2608 C9
2609 C2
2610 C8
2612 D8
2616 E7
2617 E8
2620 F6
2621 F7
2622 F5
2623 F5
2624 D1
2625 D1
2626 D1
2627 E1
3600 A8
3601 B1
3602 B9
3603 B1
3606 D2
3607 D2
4601 A5
5600 A8
5601 F5
5602 F5
6600 B8
7600 B6
C670 A2
F6001 D1
F6002 D1
F6004 D1
I600 A4
I601 A6
I602 A6
I603 A7
I604 A7
I605 B7
I606 B7
I607 D7
I609 F7
I611 F6
I612 F5
I613 F5
I619 C2
I620 C1
I622 C2
I623 B2
I624 B2

■ SCHEMATIC DIAGRAM

U model

ANALOG: POWER SUPPLY

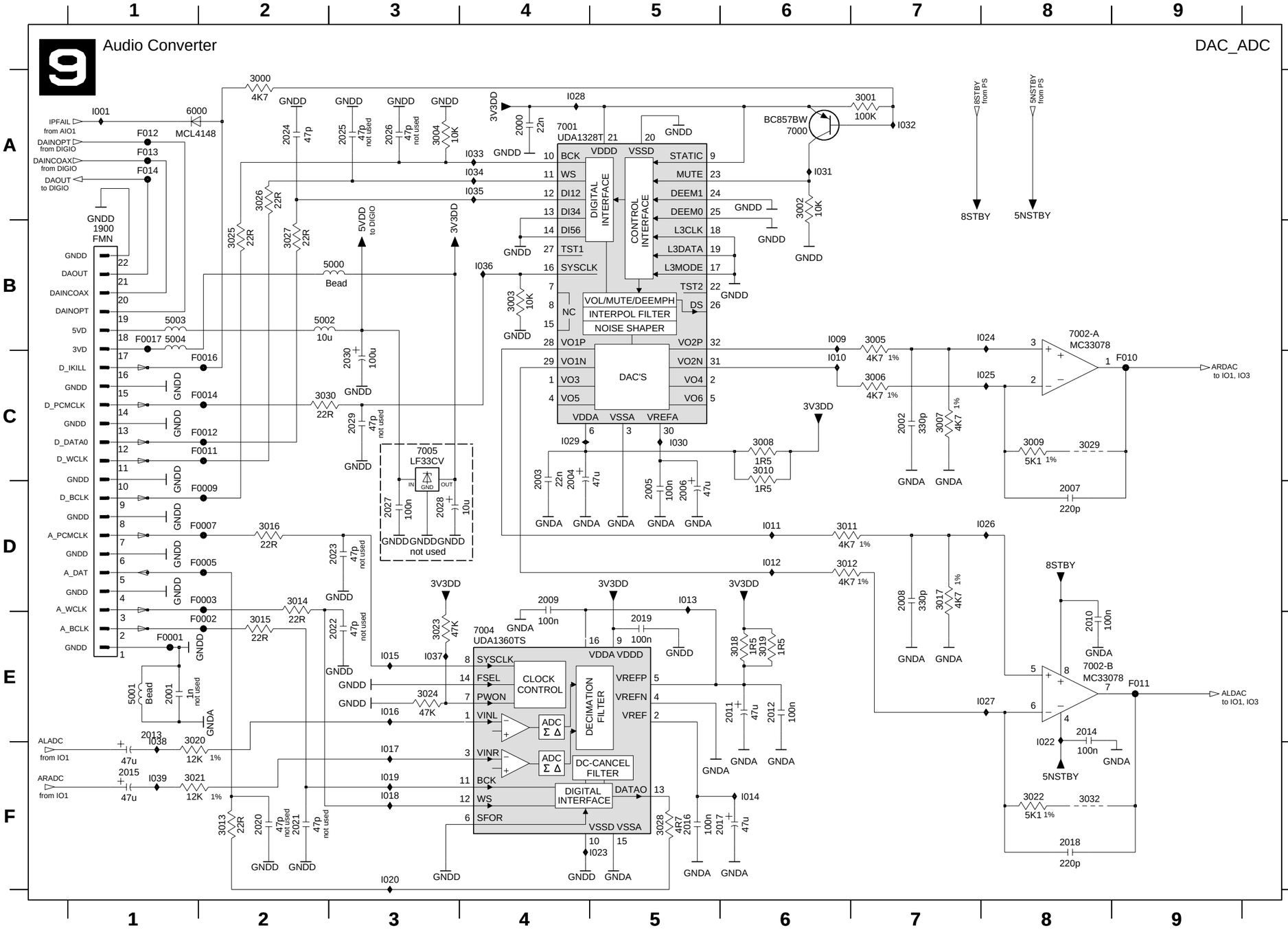


1324 E8
1325 C8
1326 B2
1327 B2
1932 C1
1996 D4
2321 C6
2322 D6
2323 D6
2324 B3
2325 B4
2328 C8
2329 E2
2330 B3
2331 B4
2332 B8
3321 C7
3322 E6
3323 F6
3325 D6
3326 D7
3335 F9
3336 F8
3337 D6
3338 D3
3339 D2
3340 E2
4320 D4
7321 C5
7322 F6
7323 D5
7324 D7
7329 F8
7330 E2
7331 E3
7332 A4
F3201 C1
F3202 C1
F3203 C1
F3204 C1
F3205 C1
F3206 D1
F3207 D1
F9330 E8
F9332 E9
F9333 E9
F9336 B6
F9338 C8
F9341 C9
F9342 C8
F9343 C8
F9344 A2
F9345 B2
F9346 C2
F9347 C2
F9349 A2
F9350 B2
I324 C6
I325 F5
I326 F6
I337 F8
I338 F8
I339 D6
I340 E2
I341 D3
I345 A4

■ SCHEMATIC DIAGRAM

U model

ANALOG: AUDIO CONVERTER



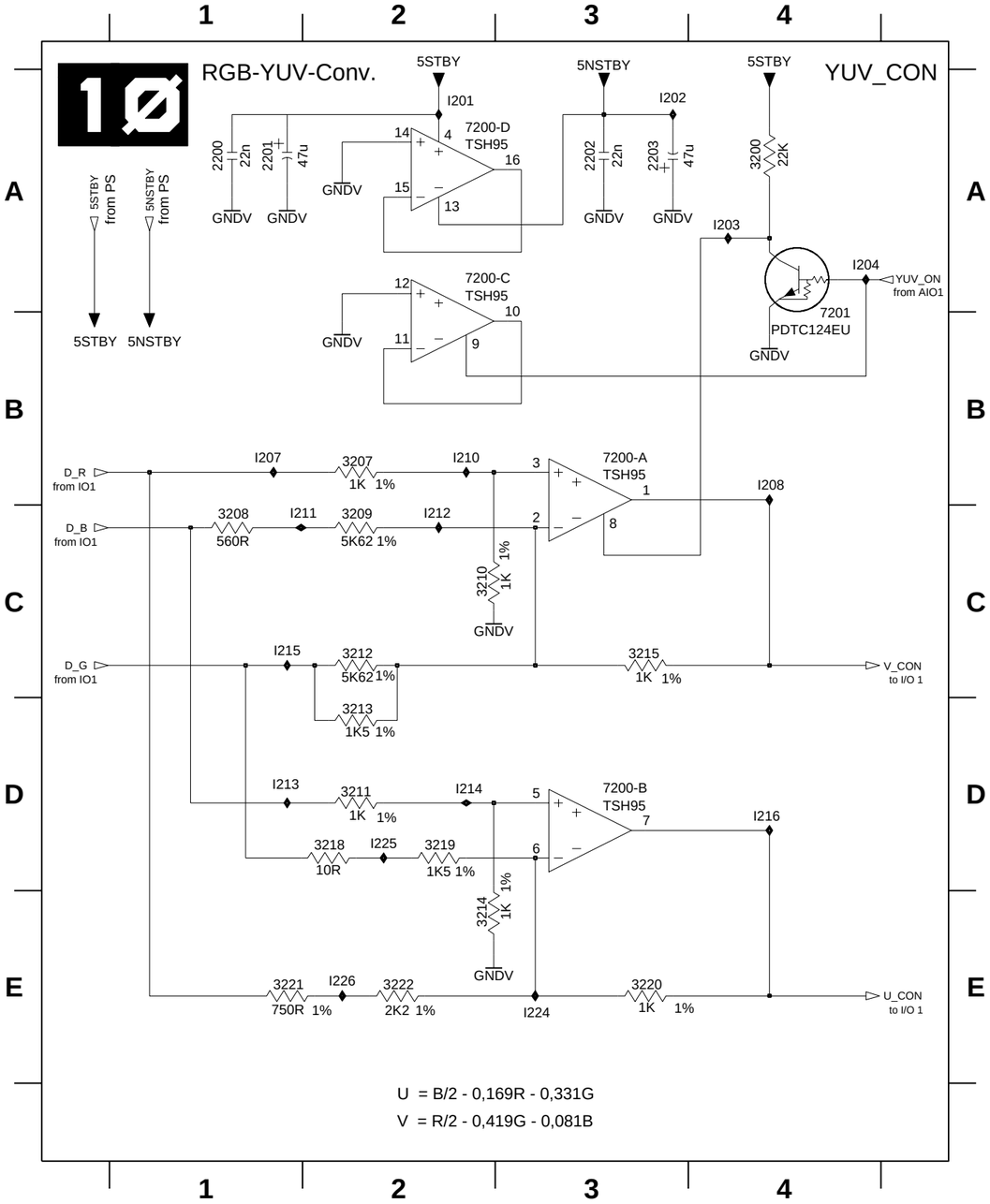
1900 B1	F0002 E2
2000 A4	F0003 D2
2001 E1	F0005 D2
2002 C7	F0007 D2
2003 C4	F0009 D2
2004 C4	F0011 C2
2005 D5	F0012 C2
2006 D5	F0014 C2
2007 D8	F0016 C2
2008 D7	F0017 B1
2009 D4	F010 C9
2010 E8	F011 E9
2011 E6	F012 A1
2012 E6	F013 A1
2013 E1	F014 A1
2014 E8	I001 A1
2015 F1	I009 B6
2016 F5	I010 C6
2017 F6	I011 D6
2018 F8	I012 D6
2019 E5	I013 D5
2020 F2	I014 F6
2021 F2	I015 E3
2022 E3	I016 E3
2023 D3	I017 F3
2024 A2	I018 F3
2025 A3	I019 F3
2026 A3	I020 F3
2027 D3	I022 E8
2028 D3	I023 F5
2029 C3	I024 B8
2030 C3	I025 C8
3000 A2	I026 D8
3001 A7	I027 E8
3002 A6	I028 A4
3003 B4	I029 C4
3004 A3	I030 C5
3005 B7	I031 A6
3006 C7	I032 A7
3007 C7	I033 A4
3008 C6	I034 A4
3009 C8	I035 A4
3010 C6	I036 B4
3011 D6	I037 E3
3012 D6	I038 F1
3013 F2	I039 F1
3014 D2	
3015 E2	
3016 D2	
3017 D7	
3018 E6	
3019 E6	
3020 F1	
3021 F1	
3022 F8	
3023 E3	
3024 E3	
3025 B2	
3026 A2	
3027 B2	
3028 F5	
3029 C8	
3030 C2	
3032 F8	
5000 B3	
5001 E1	
5002 B2	
5003 B1	
5004 B1	
6000 A1	
7000 A6	
7001 A4	
7002-A B8	
7002-B E8	
7004 E4	
7005 C3	
F0001 E1	

■ SCHEMATIC DIAGRAM

U model

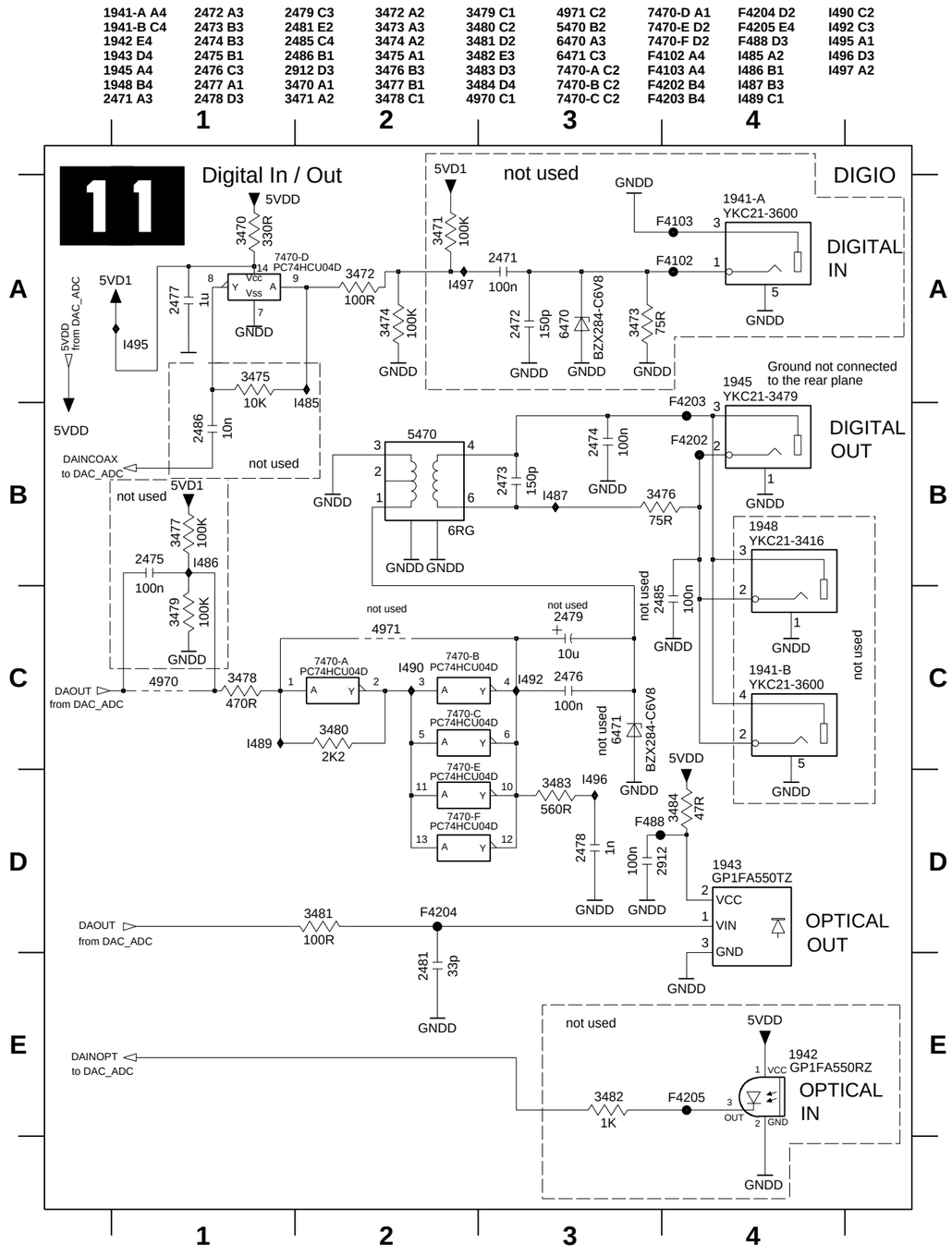
ANALOG: RGB-YUV CONVERTER

2200 A1	3200 A4	3210 C2	3214 E2	3220 E3	7200-B D3	I201 A2	I207 B1	I212 C2	I216 D4
2201 A1	3207 B2	3211 D2	3215 C3	3221 E1	7200-C A2	I202 A3	I208 B4	I213 D1	I224 E3
2202 A3	3208 C1	3212 C2	3218 D2	3222 E2	7200-D A2	I203 A4	I210 B2	I214 D2	I225 D2
2203 A3	3209 C2	3213 D2	3219 D2	7200-A B3	7201 B4	I204 A4	I211 C2	I215 C1	I226 E2



ANALOG: DIGITAL IN / OUT

1941-A A4	2472 A3	2479 C3	3472 A2	3479 C1	4971 C2	7470-D A1	F4204 D2	I490 C2
1941-B C4	2473 B3	2481 E2	3473 A3	3480 C2	5470 B2	7470-E D2	F4205 E4	I492 C3
1942 E4	2474 B3	2485 C4	3474 A2	3481 D2	6470 A3	7470-F D2	F488 D3	I495 A1
1943 D4	2475 B1	2486 B1	3475 A1	3482 E3	6471 C3	F4102 A4	I485 A2	I496 D3
1945 A4	2476 C3	2912 D3	3476 B3	3483 D3	7470-A C2	F4103 A4	I486 B1	I497 A2
1948 B4	2477 A1	3470 A1	3477 B1	3484 D4	7470-B C2	F4202 B4	I487 B3	
2471 A3	2478 D3	3471 A2	3478 C1	4970 C1	7470-C C2	F4203 B4	I489 C1	

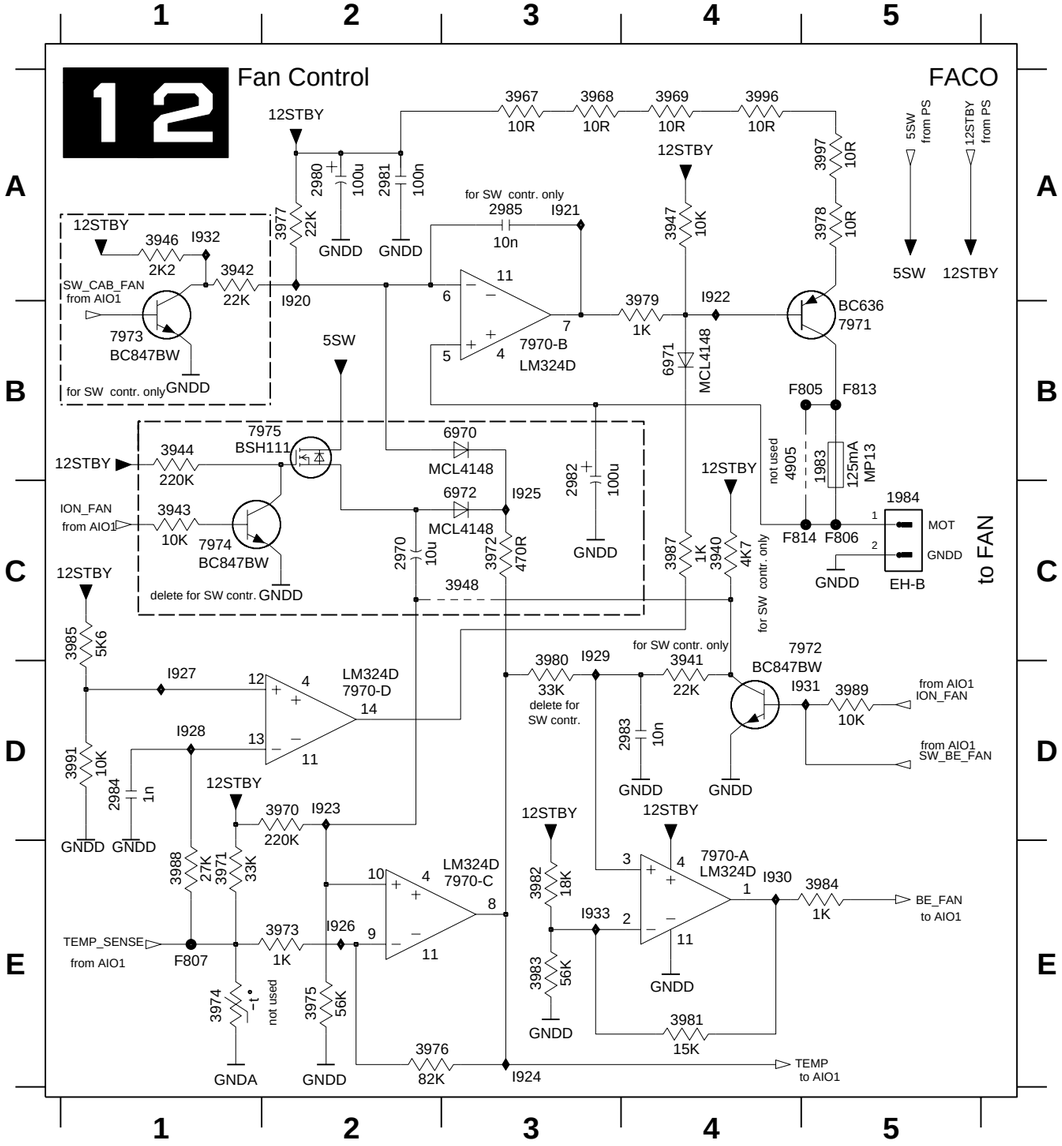


■ SCHEMATIC DIAGRAM

U model

ANALOG: FAN CONTROL

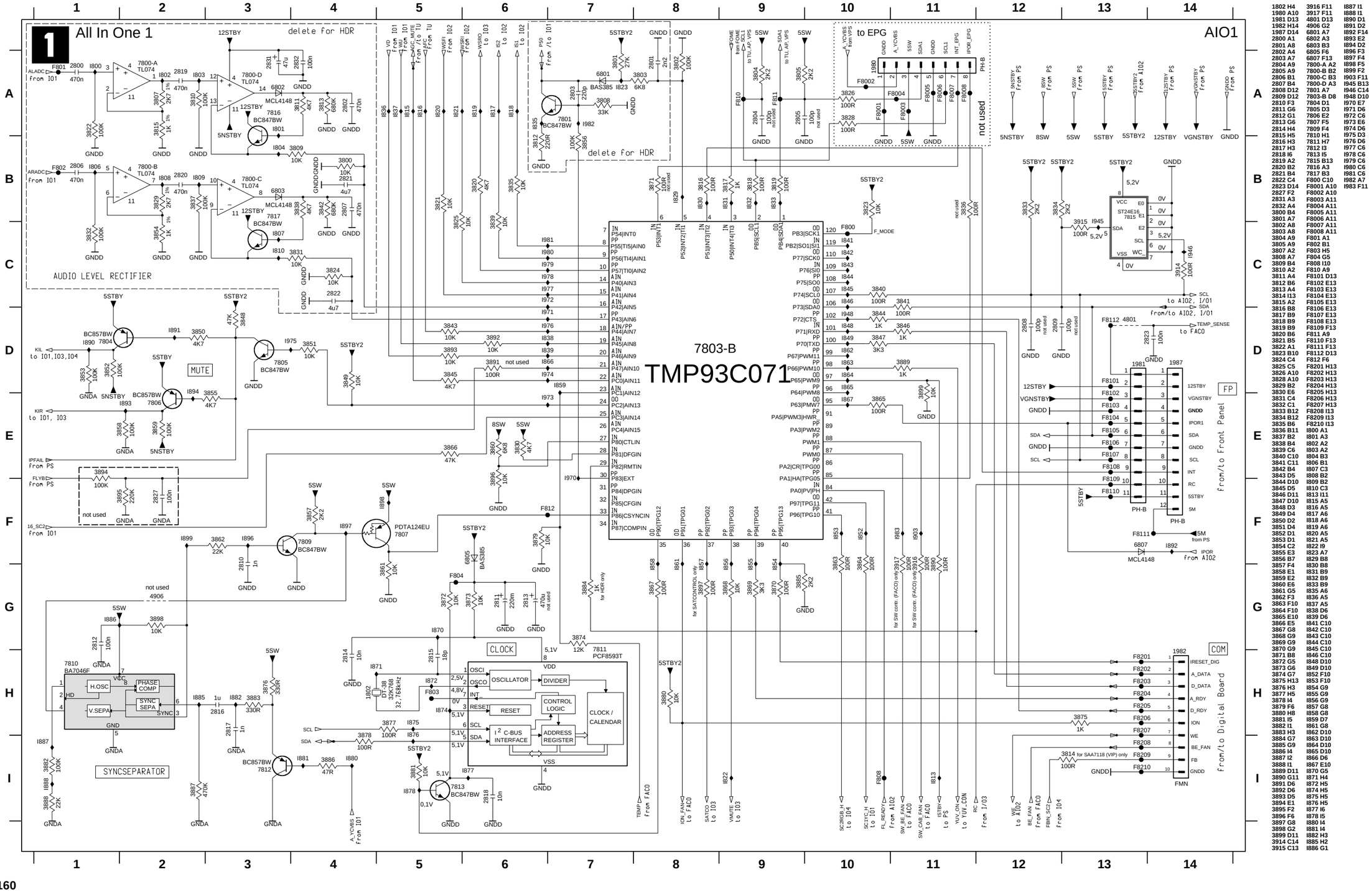
1983 B5	2985 A3	3948 C3	3974 E1	3982 E3	3996 A4	7970-C E3	F806 C5	I924 E3	I932 A1
1984 C5	3940 C4	3967 A3	3975 E2	3983 E3	3997 A5	7970-D D2	F807 E1	I925 C3	I933 E3
2970 C2	3941 D4	3968 A3	3976 E2	3984 E5	4905 B4	7971 B5	F813 B5	I926 E2	
2980 A2	3942 A1	3969 A4	3977 A2	3985 C1	6970 B3	7972 C5	F814 C4	I927 D1	
2981 A2	3943 C1	3970 D2	3978 A5	3987 C4	6971 B4	7973 B1	I920 A2	I928 D1	
2982 B3	3944 B1	3971 E1	3979 B4	3988 E1	6972 C3	7974 C1	I921 A3	I929 C3	
2983 D4	3946 A1	3972 C3	3980 D3	3989 D5	7970-A E4	7975 B2	I922 A4	I930 E4	
2984 D1	3947 A4	3973 E2	3981 E4	3991 D1	7970-B B3	F805 B5	I923 D2	I931 D5	



■ SCHEMATIC DIAGRAM

A, B, G model

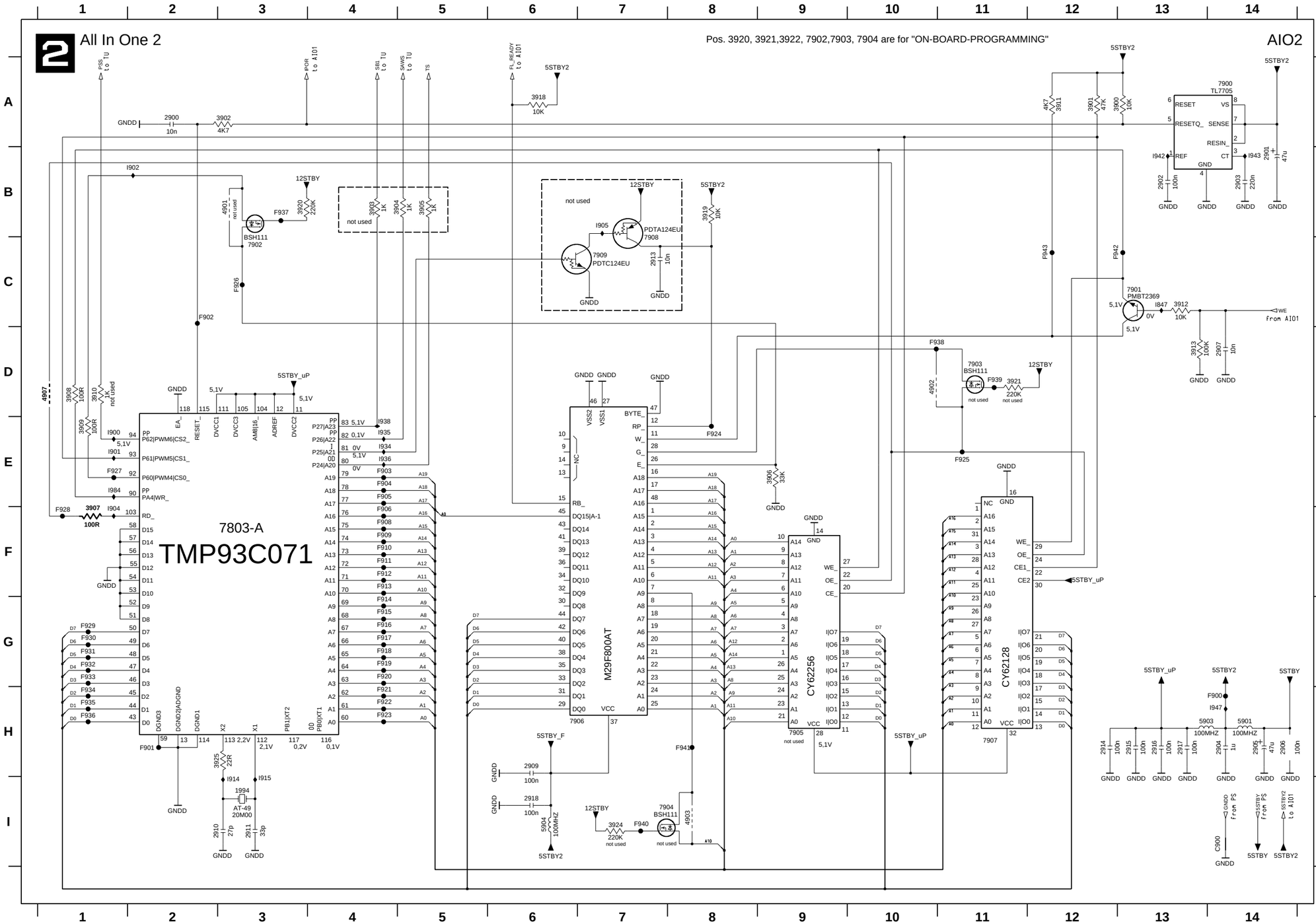
ANALOG: All in One 1


1
All In One 1
delete for HDR
AUDIO LEVEL RECTIFIER
SYNCSEPARATOR
MUTE
CLOCK
7803-B
TMP93C071
AIO1
to EPG
not used
FP
COM
PH-B
FMN
from/to Front Panel
from/to Digital Board
F801
F802
F812
F804
F803
F810
F811
F8001
F8002
F8003
F8004
F8005
F8006
F8007
F8008
F8101
F8102
F8103
F8104
F8105
F8106
F8107
F8108
F8109
F8110
F8111
F8112
F8201
F8202
F8203
F8204
F8205
F8206
F8207
F8208
F8209
F8210
F800
F808
7800-A TL074
7800-B TL074
7800-C TL074
7800-D TL074
MCL4148
BC847BW
BC857BW
BC847BW
BC847BW
BC847BW
BC847BW
BC857BW
BC857BW
PDTA124EU
BAS385
BA7046F
PCF8593T
ST24E16
PHASE COMP
SYNC SEPA
H.OSC
V.SEPA
OSCILLATOR
DIVIDER
CONTROL LOGIC
RESET
ADDRESS REGISTER
CLOCK / CALENDAR
I²C-BUS INTERFACE
32.768KHz
5,2V
0V
5,1V
2,5V
4,8V
5STBY
5STBY2
5NSTBY
12STBY
8SW
5SW
GNDD
GNDA
VGNSTBY
VD from I01
HD from I01
AGC_MUTE from/to TU
WSFI from I02
WSRO from I02
WSRO to I03
IS2 to I02
IS1 to I02
P50 from/to I01
SDA1 to TU, AP, VPS
SCL1 to TU, AP, VPS
FOME from FOME
A_YCVBS from VPS
INT_EPG
IPOR_EPG
ALADC from I01
ARADC from I01
KIL to I01,I03,I04
KIR to I01, I03
IPFAIL from PS
FLYB from PS
16_SC2 from I01
A_YCVBS from I01
TEMP from FACO
ION_FAN to FACO
SATCO to I03
VMUTE to I03
SC2RGB_H to I04
SC1VC_H to I01
FL_READY from A102
SW_BE_FAN to FACO
SW_CAB_FAN to FACO
ISTBY to PS
YUV_CON to YUV_CON
RC from I/O3
WR to A102
BE_FAN from FACO
FBN_SC2 from I04
SCL to A102, I/O1
SDA from/to A102, I/O1
TEMP_SENSE to FACO
IRESET_DIG
A_DATA
D_DATA
A_RDY
D_RDY
ION
WE
BE_FAN
FB
IPOR1
INT
RC
IPOR from A102
5M from PS
F_MODE
SW contr. (FACO) only
for SATCONTROL only
for HDR only
not used
not used, not used
not used, not used
not used,

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: All in One 2



1994 I3
2900 A2
2901 B14
2902 B13
2903 B14
2904 H14
2905 H14
2906 H14
2907 D14

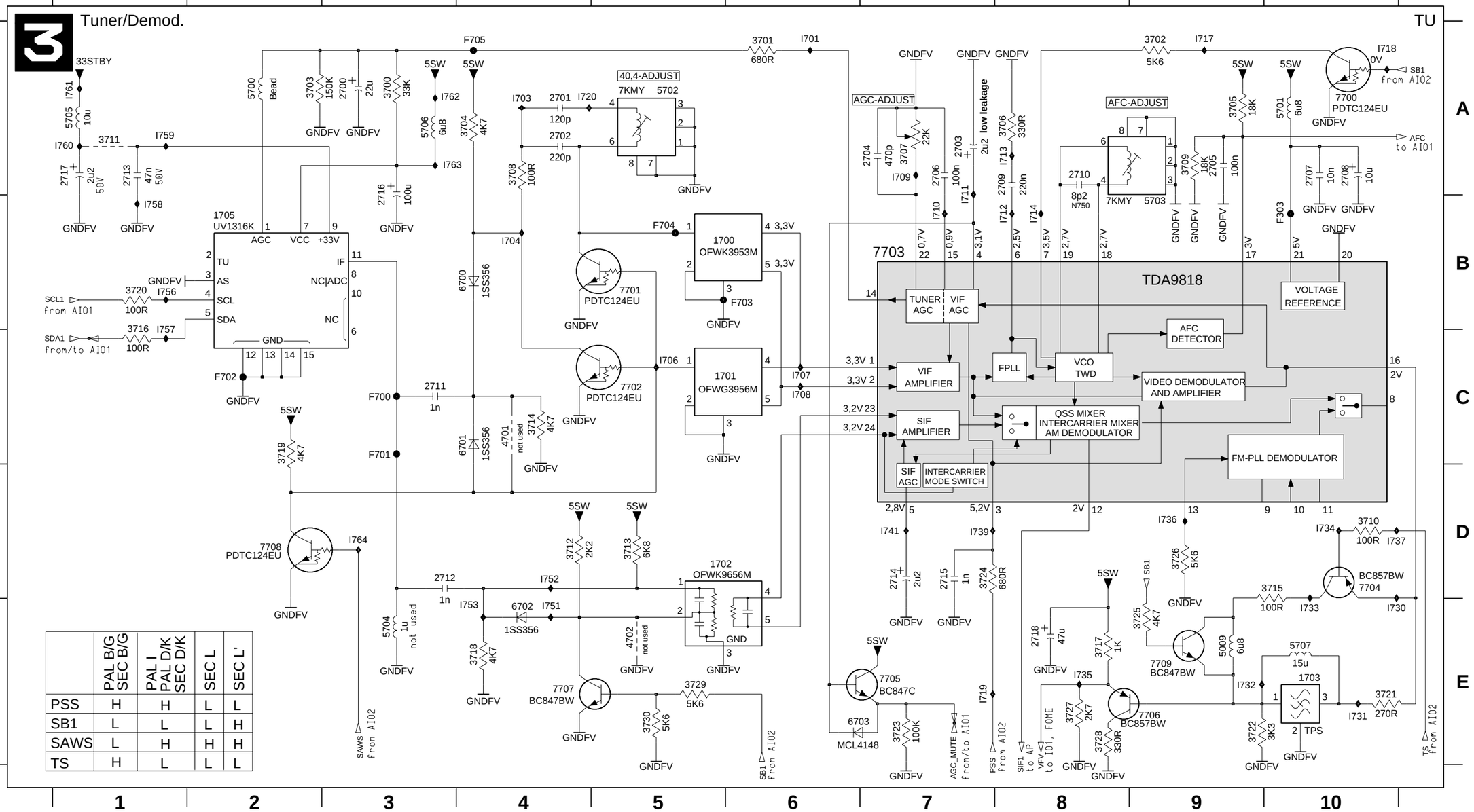
2909 H6
2910 I3
2911 I3
2913 C7
2914 H12
2915 H13
2916 H13
2917 H13
2918 I6
3900 A13
3901 A12
3902 A3
3903 B4
3904 B5
3905 B5
3906 E9
3907 E1
3908 D1
3909 E1
3910 D1
3911 A12
3912 C13
3913 D13
3918 A6
3919 B8
3920 B3
3921 D11
3924 I7
3925 H3
4901 B3
4902 D10
4903 I8
4907 D1
5901 H14
5903 H13
5904 I6
7803-A F3
7900 A14
7901 C13
7902 C3
7903 D11
7904 I7
7905 H9
7906 H7
7907 H11
7908 B7
7909 C7
C900 I14
F900 H14
F901 H2
F902 C2
F903 E4
F904 E4
F905 E4
F906 F4
F908 F4
F909 F4
F910 F4
F911 F4
F912 F4
F913 F4
F914 G4
F915 G4
F916 G4
F917 G4
F918 G4
F919 G4
F920 G4
F921 H4
F922 H4
F923 H4
F924 E8
F925 E11
F926 C3
F927 E1
F928 F1
F929 G1
F930 G1
F931 G1
F932 G1
F933 G1
F934 H1
F935 H1
F936 H1
F937 B3
F938 D10
F939 D11
F940 I7
F941 H8
F942 C13
F943 C12
I847 C13
I900 E1
I901 E1
I902 B2
I904 F1
I905 B7
I914 I3
I915 I3
I934 E4
I935 E4
I936 E4
I938 E4
I942 B13
I943 B14
I947 H14
I984 E1

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: TUNER / DEMODULATOR

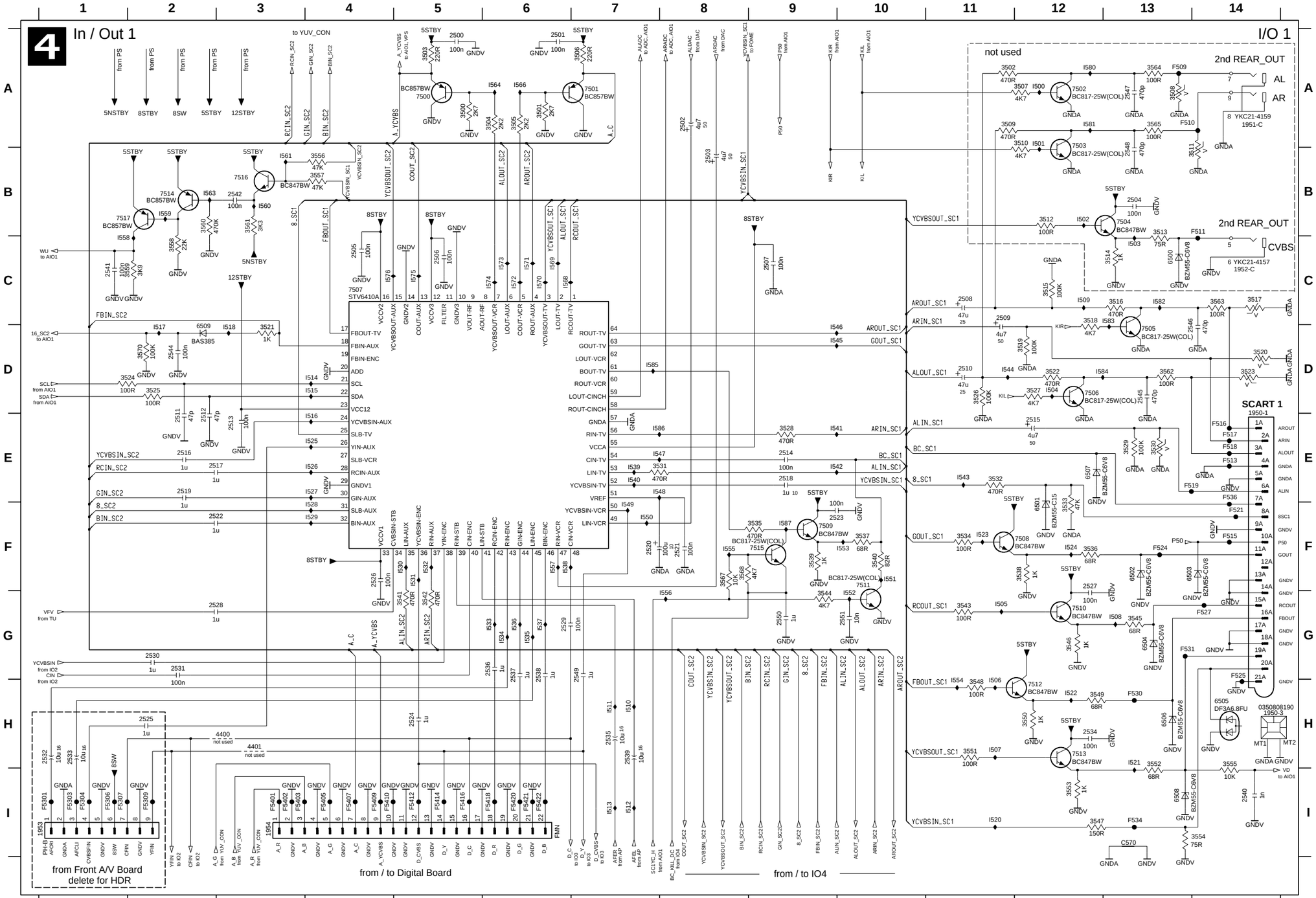
1700 B5	2700 A3	2705 A9	2710 A8	2715 D7	3701 A6	3706 A8	3711 A1	3716 C1	3721 E10	3726 D9	4701 C4	5702 A5	5707 E10	7700 A10	7705 E7	F303 B10	F704 B5	I706 C5	I711 A7	I718 A10	I732 E9	I737 D10	I753 E4	I760 A1
1701 C5	2701 A4	2706 A7	2711 C3	2716 A3	3702 A9	3707 A7	3712 D4	3717 E8	3722 E9	3727 E8	4702 E5	5703 B9	6700 B4	7701 B5	7706 E9	F700 C3	F705 A4	I707 C6	I712 B8	I719 E7	I733 E10	I739 D7	I756 B1	I761 A1
1702 D5	2702 A4	2707 A10	2712 D3	2717 A1	3703 A2	3708 A4	3713 D5	3718 E4	3723 E7	3728 E8	5009 E9	5704 E3	6701 C4	7702 C5	7707 E4	F701 C3	I701 A6	I708 C6	I713 A8	I720 A4	I734 D10	I741 D7	I757 B1	I762 A3
1703 E10	2703 A7	2708 A10	2713 A1	2718 E8	3704 A4	3709 A9	3714 C4	3719 C2	3724 D7	3729 E5	5700 A2	5705 A1	6702 E4	7703 B7	7708 D2	F702 C2	I703 A4	I709 A7	I714 B8	I730 E10	I735 E8	I751 E4	I758 B1	I763 A3
1705 B2	2704 A7	2709 A8	2714 D7	3700 A3	3705 A9	3710 D10	3715 D10	3720 B1	3725 E9	3730 E5	5701 A10	5706 A3	6703 E6	7704 D10	7709 E9	F703 B6	I704 B4	I710 B7	I717 A9	I731 E10	I736 D9	I752 D4	I759 A1	I764 D3



■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: IN /OUT 1

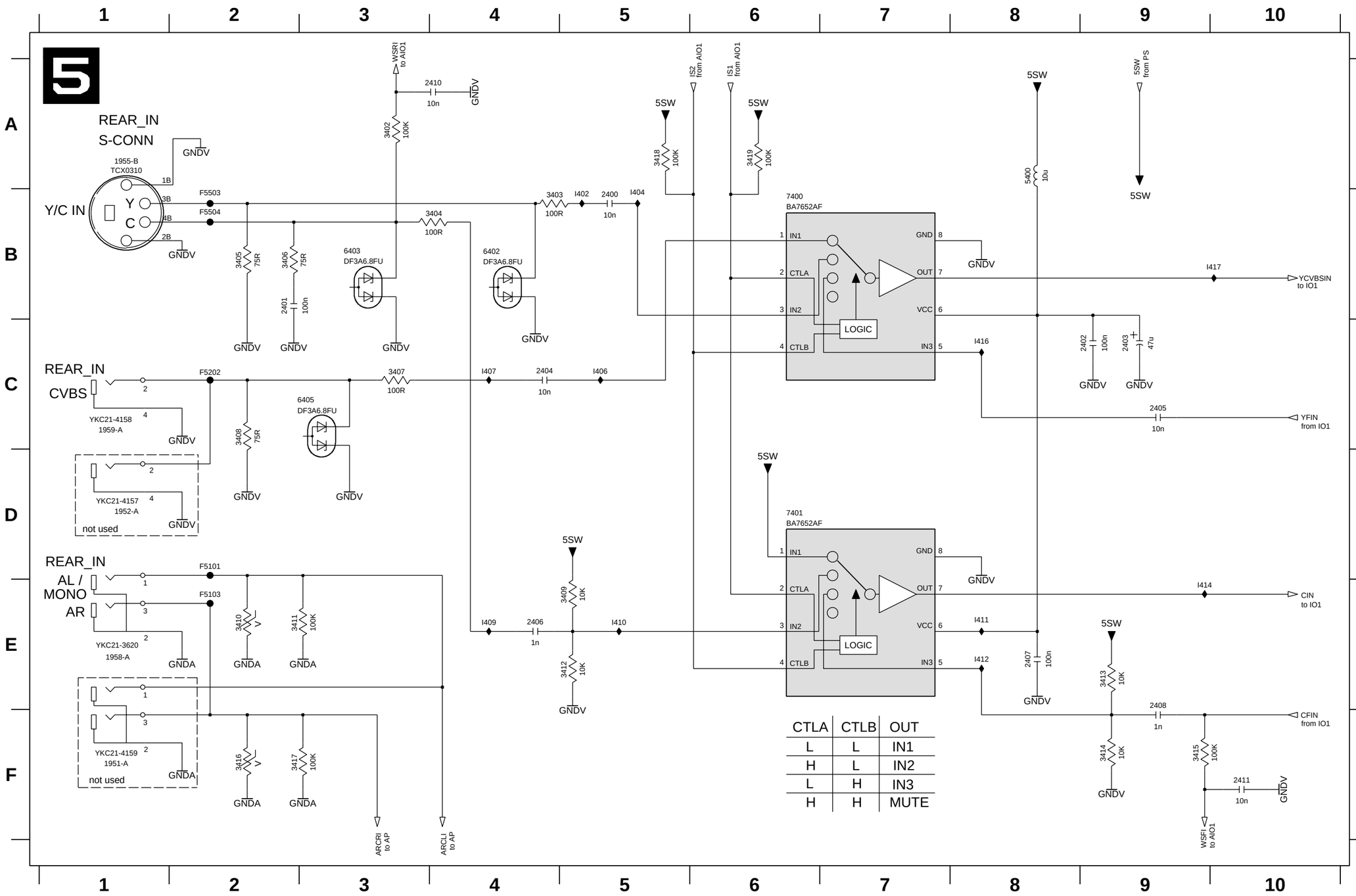


1950-1 E14	3560 B2	I541 E9
1950-3 H14	3561 B3	I542 E9
1951-C A14	3562 D13	I543 E11
1952-C C14	3563 C14	I544 D11
1953 I1	3564 A13	I545 D9
1954 I3	3565 A13	I546 D9
2500 A5	3567 F8	I547 E7
2501 A6	3568 F8	I548 E7
2502 A8	3570 D2	I549 F7
2503 B8	4400 H3	I550 F7
2504 B13	4401 H3	I551 F10
2505 C4	6500 C13	I552 G10
2506 C5	6501 F12	I553 F10
2507 C9	6502 F13	I554 H11
2508 C11	6503 F13	I555 G8
2509 C11	6504 G13	I556 F8
2510 D11	6505 H14	I557 F6
2511 E2	6506 H13	I558 C1
2512 E2	6507 E12	I559 B2
2513 E3	6508 I13	I560 B3
2514 E9	6509 D2	I561 B3
2515 E12	7500 A5	I563 B2
2516 E2	7501 A7	I564 A6
2517 E2	7502 A12	I566 A6
2518 E9	7503 B12	I568 C6
2519 E2	7504 B13	I569 C6
2520 F7	7505 D13	I570 C6
2521 F8	7506 D12	I571 C6
2522 F2	7507 C4	I572 C6
2523 F9	7508 F12	I573 C6
2524 H5	7509 F9	I574 C6
2525 H2	7510 G12	I575 C5
2526 F4	7511 F10	I576 C4
2527 F12	7512 H12	I580 A12
2528 G2	7513 H12	I581 A12
2529 G6	7514 B2	I582 C13
2530 G2	7515 F9	I583 C13
2531 G2	7516 B3	I584 D12
2532 H1	7517 B2	I585 D7
2533 H1	C570 I13	I586 E7
2534 H12	F509 A13	I587 F9
2535 H7	F510 A13	
2536 G6	F511 B14	
2537 G6	F513 E14	
2538 G6	F515 F14	
2539 H7	F516 E14	
2540 I14	F517 E14	
2541 C1	F518 E14	
2542 B3	F519 E13	
2544 D2	F521 F14	
2545 D13	F524 F13	
2546 D14	F525 G14	
2547 A13	F527 G14	
2548 B13	F530 H13	
2549 G7	F531 I1	
2550 G9	F5303 I1	
2551 G10	F5304 I1	
3500 A5	F5306 I1	
3501 A6	F5307 I1	
3502 A11	F5309 I2	
3503 A5	F531 G13	
3504 A6	F534 I13	
3505 A6	F536 E14	
3506 A7	F5401 I3	
3507 A12	F5402 I3	
3508 A13	F5403 I3	
3509 A11	F5405 I4	
3510 A12	F5407 I4	
3511 B14	F5409 I4	
3512 B12	F5410 I4	
3513 B13	F5412 I5	
3514 C13	F5414 I5	
3515 C12	F5416 I5	
3516 C13	F5418 I6	
3517 C14	F5420 I6	
3518 C12	F5421 I6	
3519 D12	F5422 I6	
3520 D14	I500 A12	
3521 D3	I501 A12	
3522 D12	I502 B12	
3523 D14	I503 C13	
3524 D2	I504 D12	
3525 D2	I505 G11	
3526 D11	I506 H11	
3527 D12	I507 H11	
3528 E9	I508 G13	
3529 E13	I509 C12	
3530 E13	I510 H7	
3531 E8	I511 H7	
3532 E11	I512 I7	
3533 F12	I513 I7	
3534 F11	I514 D4	
3535 F9	I515 D4	
3536 F12	I516 E4	
3537 F10	I517 D2	
3538 F12	I518 D3	
3539 F9	I520 I11	
3540 F10	I521 H13	
3541 G5	I522 H12	
3542 G5	I523 F11	
3543 G11	I524 F12	
3544 G9	I525 E4	
3545 G13	I526 E4	
3546 G12	I527 E4	
3547 I12	I528 F4	
3548 H11	I529 F4	
3549 H12	I530 F5	
3550 H12	I531 F5	
3551 H11	I532 F5	
3552 H13	I533 G6	
3553 I12	I534 G6	
3554 I14	I535 G6	
3555 H14	I536 G6	
3556 B4	I537 G6	
3557 B4	I538 F6	
3558 C2	I539 E7	
3559 C2	I540 E7	

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: IN /OUT 2



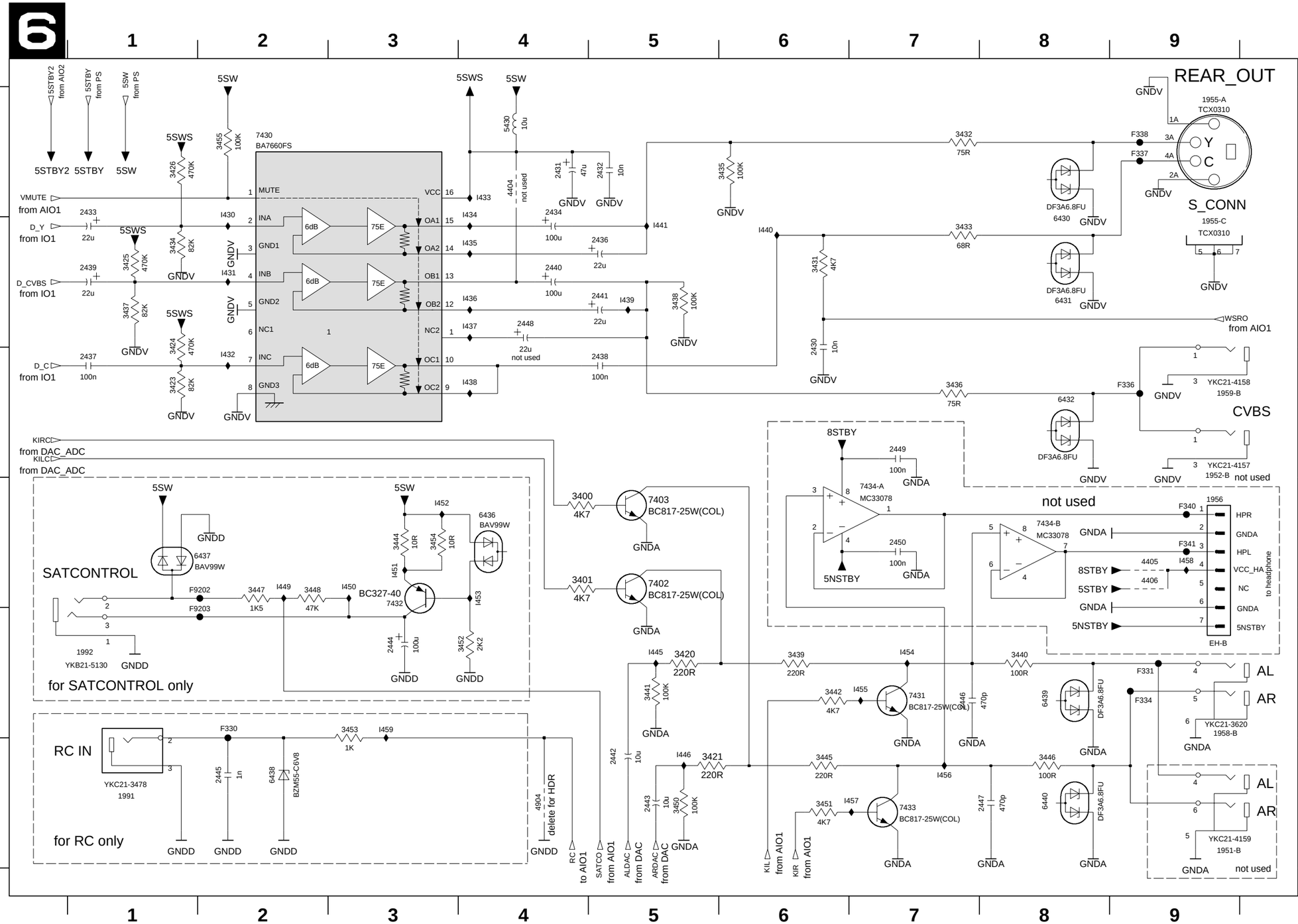
CTLA	CTLB	OUT
L	L	IN1
H	L	IN2
L	H	IN3
H	H	MUTE

1951-A F1
1952-A D1
1955-B A1
1958-A E1
1959-A C1
2400 B5
2401 B2
2402 C9
2403 C9
2404 C4
2405 C9
2406 E4
2407 E8
2408 E9
2410 A4
2411 F10
3402 A3
3403 B4
3404 B4
3405 B2
3406 B2
3407 C3
3408 C2
3409 E5
3410 E2
3411 E2
3412 E5
3413 E9
3414 F9
3415 F9
3416 F2
3417 F2
3418 A5
3419 A6
5400 A8
6402 B4
6403 B3
6405 C2
7400 B6
7401 D6
F5101 D2
F5103 E2
F5202 C2
F5503 B2
F5504 B2
I402 B5
I404 B5
I406 C5
I407 C4
I409 E4
I410 E5
I411 E8
I412 E8
I414 E9
I416 C8
I417 B10

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: IN /OUT 3

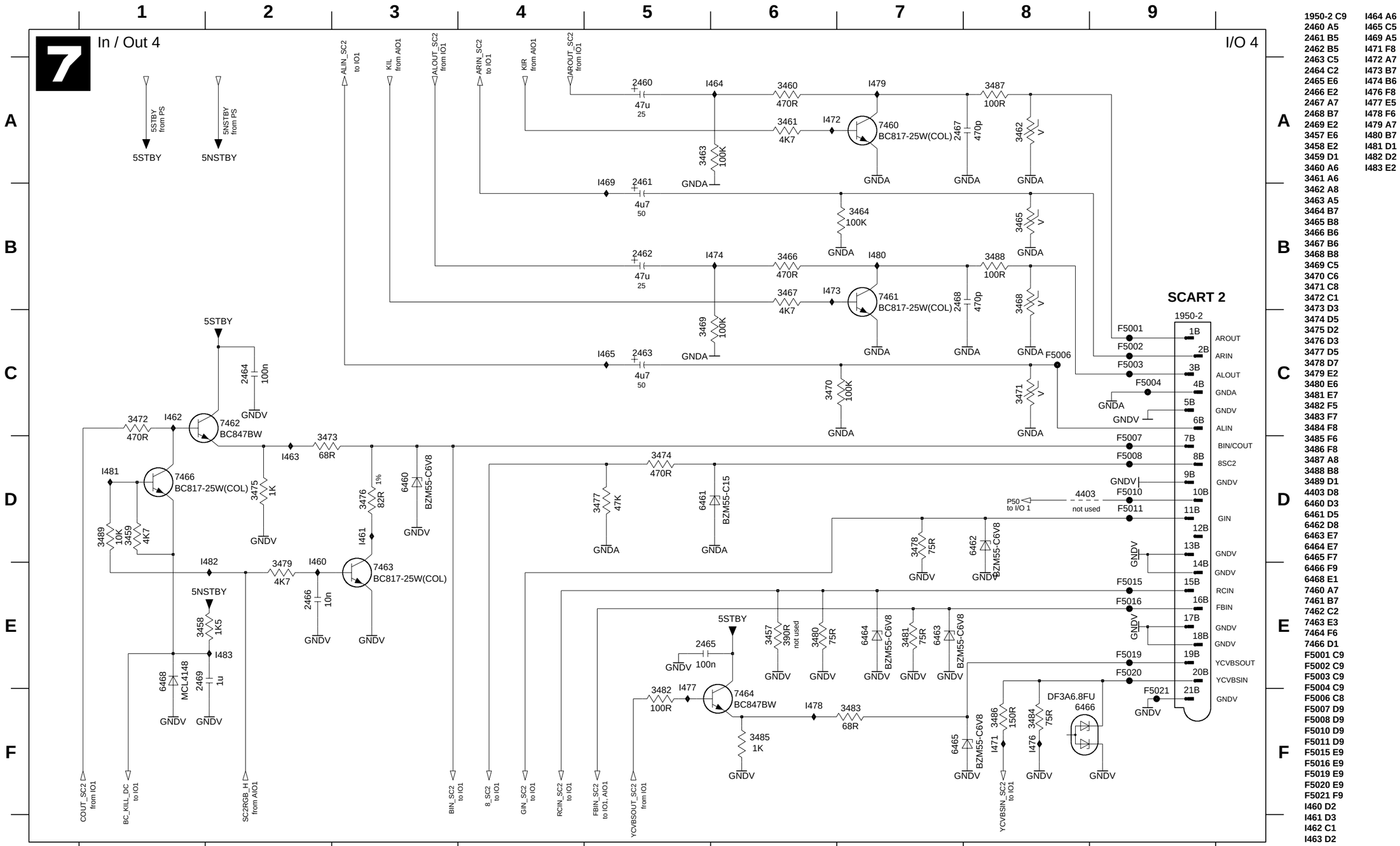


1951-B F9
1952-B C9
1955-A A9
1955-C B9
1956 D9
1958-B E9
1959-B C9
1991 F1
1992 E1
2430 B6
2431 A4
2432 A5
2433 A1
2434 A4
2436 B5
2437 C1
2438 C5
2439 B1
2440 B4
2441 B5
2442 F5
2443 F5
2444 E3
2445 F2
2446 E7
2447 F8
2448 B4
2449 C7
2450 D7
3400 D4
3401 D4
3420 E5
3421 F5
3423 C1
3424 B1
3425 B1
3426 A1
3431 B6
3432 A7
3433 B7
3434 B1
3435 A6
3436 C7
3437 B1
3438 B5
3439 E6
3440 E8
3441 E5
3442 E5
3444 D3
3445 F6
3446 F8
3447 D2
3448 D2
3450 F5
3451 F6
3452 E4
3453 E3
3454 D3
3455 A2
4404 A4
4405 D9
4406 D9
4904 F4
5430 A4
6430 A8
6431 B8
6432 C8
6436 D4
6437 D1
6438 F2
6439 E8
6440 F8
7402 D5
7403 D5
7430 A2
7431 E7
7432 D3
7433 F7
7434-A D7
7434-B D8
F330 E2
F331 E9
F334 E9

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: IN /OUT 4



1950-2 C9
2460 A5
2461 B5
2462 B5
2463 C5
2464 C2
2465 E6
2466 E2
2467 A7
2468 B7
2469 E2
3457 E6
3458 E2
3459 D1
3460 A6
3461 A6
3462 A8
3463 A5
3464 B7
3465 B8
3466 B6
3467 B6
3468 B8
3469 C5
3470 C6
3471 C8
3472 C1
3473 D3
3474 D5
3475 D2
3476 D3
3477 D5
3478 D7
3479 E2
3480 E6
3481 E7
3482 F5
3483 F7
3484 F8
3485 F6
3486 F8
3487 A8
3488 B8
3489 D1
4403 D8
6460 D3
6461 D5
6462 D8
6463 E7
6464 E7
6465 F7
6466 F9
6468 E1
7460 A7
7461 B7
7462 C2
7463 E3
7464 F6
7466 D1
F5001 C9
F5002 C9
F5003 C9
F5004 C9
F5006 C8
F5007 D9
F5008 D9
F5010 D9
F5011 D9
F5015 E9
F5016 E9
F5019 E9
F5020 E9
F5021 F9
I460 D2
I461 D3
I462 C1
I463 D2
I464 A6
I465 C5
I469 A5
I471 F8
I472 A7
I473 B7
I474 B6
I476 F8
I477 E5
I478 F6
I479 A7
I480 B7
I481 D1
I482 D2
I483 E2

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: SOUND PROCESSING

8 Sound Processing

AP

from PS: 8SW, 5SW

C670

GNDA, GNDD

I600, 4601

2600 10u, 2601 10n, I601, I602, 2602 10u, I603, 2603 100n

I604, 3600 10K, 5SW, 5600 10u, 2604 10n, GNDD

from/to A101: SCL1, SDA1

3601 100R, 3603 100R, I624, I623

QFP44

ADR_CL, ADR_SEL, D_CTR_IO1, D_CTR_IO0, TESTEN, VREFTOP, AHVSUP, CAPL_M

I2C_CL, I2C_DA, I2S_CL, I2S_WS, I2S_DA_OUT, I2S_DA_IN1, I2S_DA_IN2

7600 MSP3415G

STBYQ, DVSUP, RESETQ

I605, I606

2605 10u, 2606 10n, GNDD

6600 MCL4148, 3602 4K7, 2608 10u, GNDD

GNDA, 2607 56p, I622, I620, 2609 56p, I619

SIF1 from TU

ANA_IN-, ANA_IN+

DEMODULATOR

S1...4, I2SL/R, I2SL/R

FM1, FM2, NICAM A, NICAM B

LOUDSPEAKER R, LOUDSPEAKER L

D/A, D/A

DACM_R, DACM_L

LOUDSPEAKER

delete for HDR

1960, EH-B

DVAR, GND, GND, DVAL

from DV - Board

F6001, F6002, F6004, GNDA

2624 2u2, 2625 2u2

3606 1K, 3607 1K

MONO_IN, SC1_IN_R, SC1_IN_L, SC2_IN_R, SC2_IN_L

IDENT, IDENT

DFP

A/D, A/D

SCART-L, SCART-R

HEADPHONE R, HEADPHONE L

SCART-R, SCART-L

D/A, D/A

SC1_OUT_R, SC1_OUT_L

AFER to IO1, AFEL to IO1

2616 1n not used, 2617 1n not used, GNDA

AGNDC, I607, 2610 10n, 2612 4u7, GNDA

ARCRI from IO2, 2614 2u2, I616, 3604 1K, I617, I614

ARCLI from IO2, 2615 2u2, I615, 3605 1K

SCART Switching Facilities

VREF2, VREF1, AHVSS, ASG, AVSS, DVSS, NC, AVSUP, TP, XTAL_IN, XTAL_OUT

GNDA, GNDD

5SW, 5601 100u, I613, 5602 10u, I612

2622 10u, 2623 10n, GNDA, GNDA

1600 HC-49/U 18M432, I611, I609

2620 3p3, 2621 3p3, GNDD, GNDD

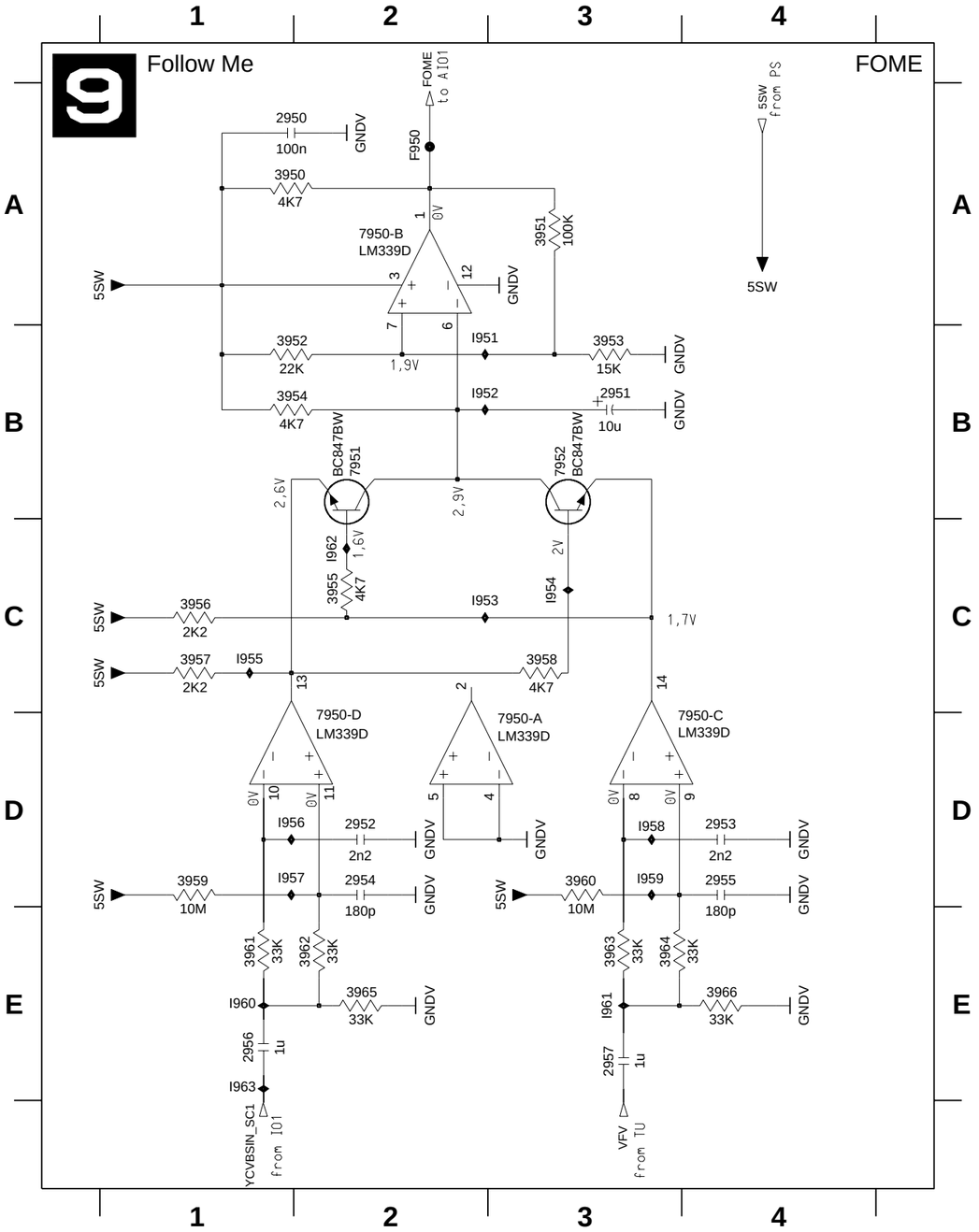
1600 F7
1960 D1
2600 A6
2601 A6
2602 A7
2603 A7
2604 A9
2605 B8
2606 B8
2607 C2
2608 C9
2609 C2
2610 C8
2612 D8
2614 E1
2615 E1
2616 E8
2617 E8
2620 F7
2621 F7
2622 F5
2623 F6
2624 D2
2625 D2
3600 A8
3601 B1
3602 B9
3603 B2
3604 E2
3605 E2
3606 D2
3607 D2
4601 A5
5600 A8
5601 F5
5602 F6
6600 B9
7600 B6
C670 A3
F6001 D1
F6002 D1
F6004 D1
I600 A4
I601 A6
I602 A7
I603 A7
I604 A8
I605 B7
I606 B7
I607 D8
I609 F7
I611 F7
I612 F6
I613 F5
I614 E2
I615 E2
I616 E2
I617 E2
I619 C2
I620 C1
I622 C2
I623 B2
I624 B2

■ SCHEMATIC DIAGRAM

A, B, G model

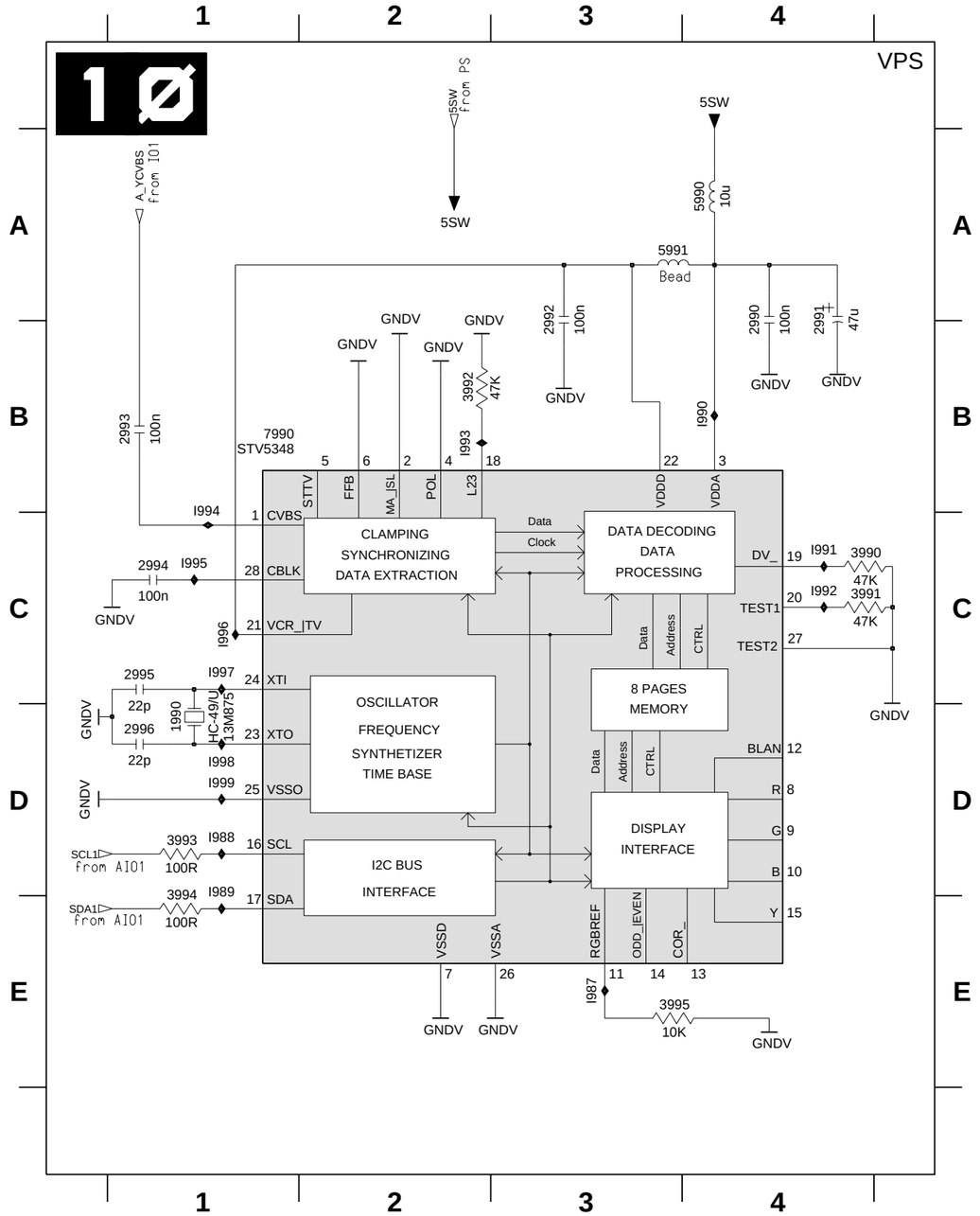
ANALOG: FOLLOW ME

2950 A1	2954 D2	3950 A1	3954 B1	3958 C3	3962 E2	3966 E4	7950 D4	I951 B2	I955 C1	I959 D3	I963 E1	
2951 B3	2955 D4	3951 A3	3955 C2	3959 D1	3963 E3	7950 A2	7951 B2	I952 B2	I956 D1	I960 E1		
2952 D2	2956 E1	3952 B1	3956 C1	3960 D3	3964 E3	7950 D2	7952 B3	I953 C2	I957 D1	I961 E3		
2953 D4	2957 E3	3953 B3	3957 C1	3961 E1	3965 E2	7950 D2	F950 A3	I954 C3	I958 D3	I962 C2		



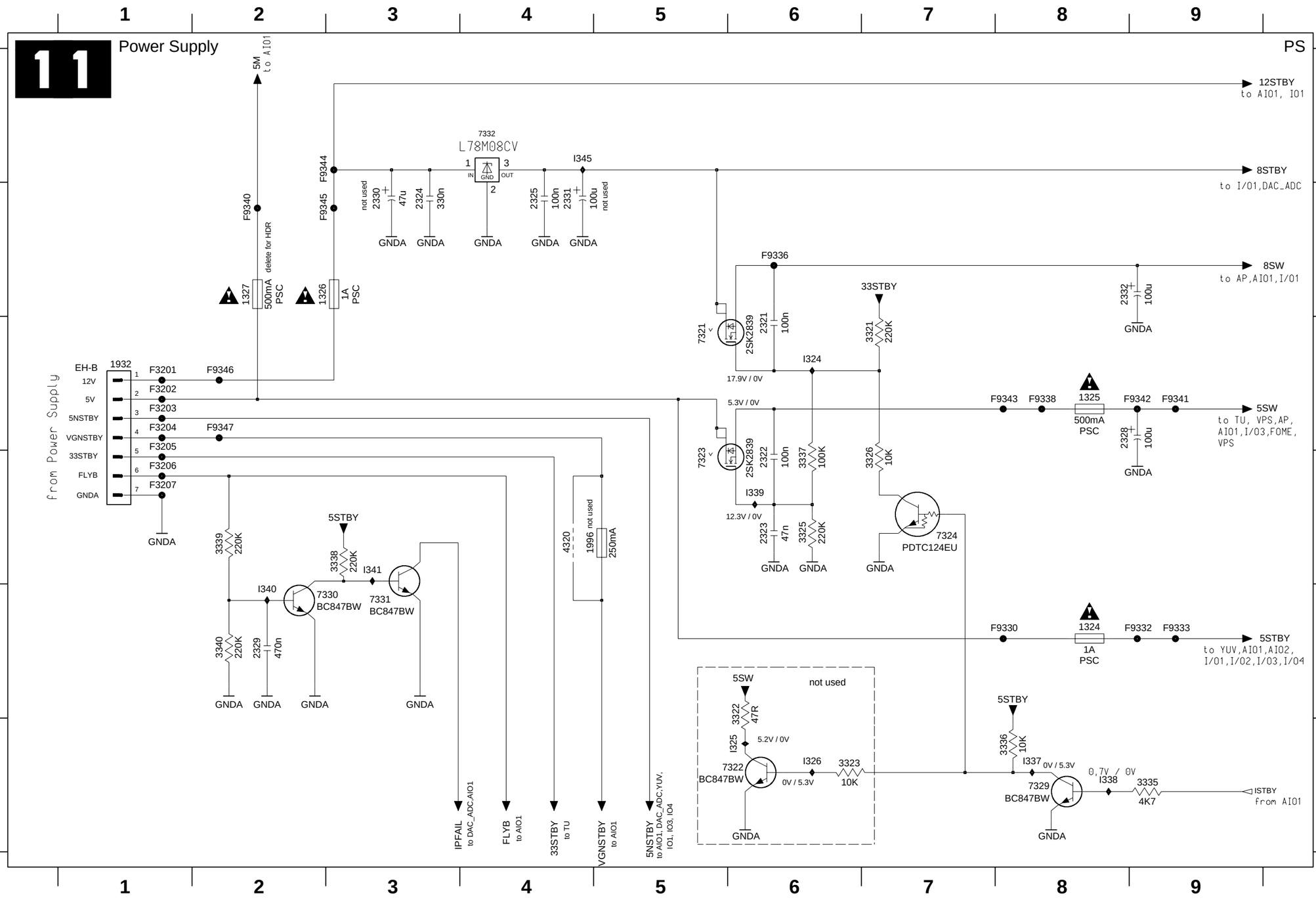
ANALOG: VPS

1990 D1	2992 A3	2995 C1	3991 C4	3994 E1	5991 A3	I988 D1	I991 C4	I994 B1	I997 C1			
2990 A4	2993 B1	2996 D1	3992 B2	3995 E3	7990 B1	I989 D1	I992 C4	I995 C1	I998 D1			
2991 A4	2994 C1	3990 C4	3993 D1	5990 A4	I987 E3	I990 B4	I993 B2	I996 C1	I999 D1			



■ SCHEMATIC DIAGRAM **A, B, G model**

ANALOG: POWER SUPPLY



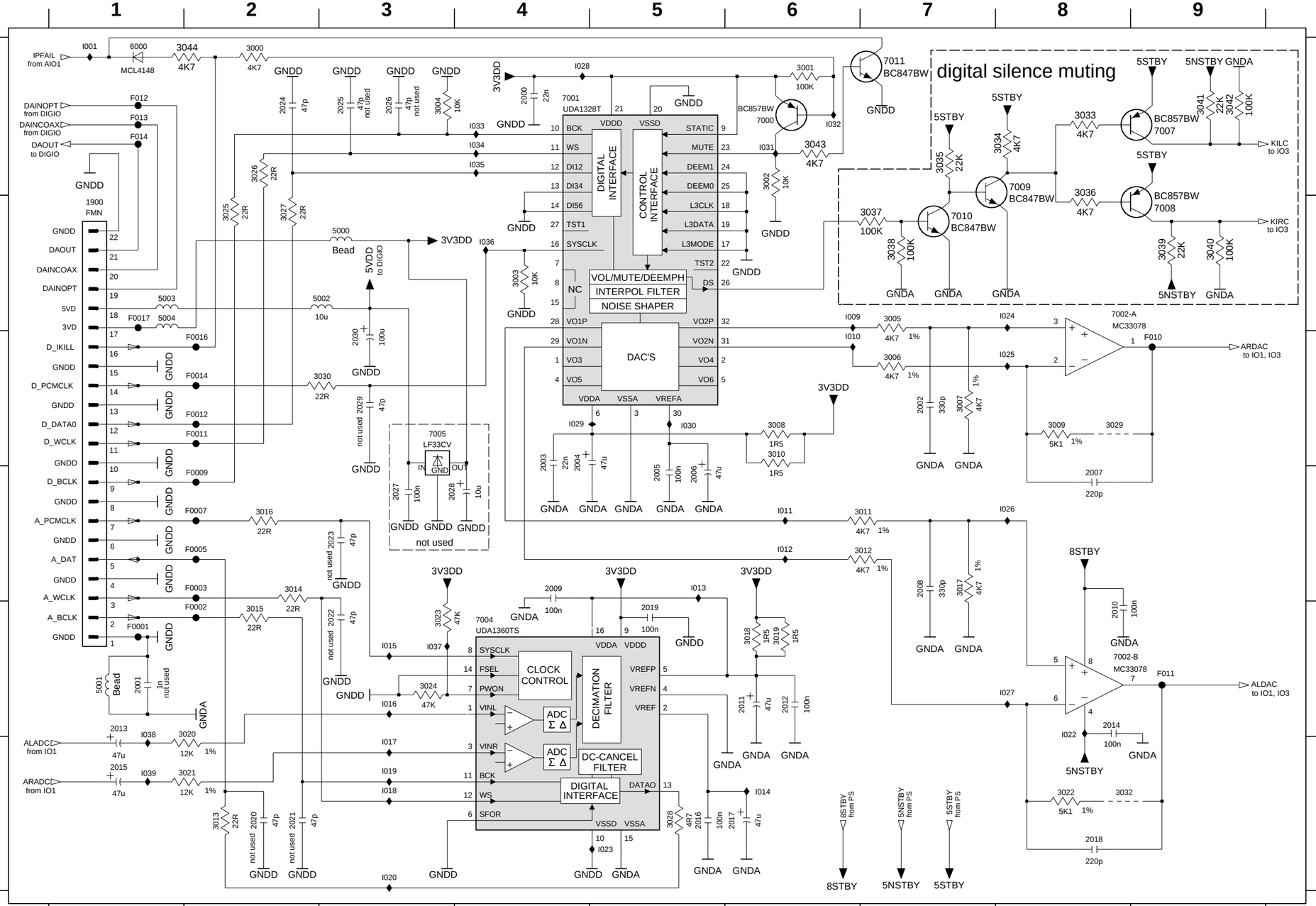
1324 E8
1325 C8
1326 B2
1327 B2
1932 C1
1996 D4
2321 C6
2322 D6
2323 D6
2324 B3
2325 B4
2328 C8
2329 E2
2330 B3
2331 B4
2332 B8
3321 C7
3322 E6
3323 F6
3325 D6
3326 D7
3335 F9
3336 F8
3337 D6
3338 D3
3339 D2
3340 E2
4320 D4
7321 C5
7322 F6
7323 D5
7324 D7
7329 F8
7330 E2
7331 E3
7332 A4
F3201 C1
F3202 C1
F3203 C1
F3204 C1
F3205 C1
F3206 D1
F3207 D1
F9330 E8
F9332 E9
F9333 E9
F9336 B6
F9338 C8
F9340 B2
F9341 C9
F9342 C9
F9343 C8
F9344 A3
F9345 B3
F9346 C2
F9347 C2
I324 C6
I325 F6
I326 F6
I337 F8
I338 F8
I339 D6
I340 E2
I341 D3
I345 A4

■ SCHEMATIC DIAGRAM

A, B, G model

ANALOG: AUDIO CONVERTER

12



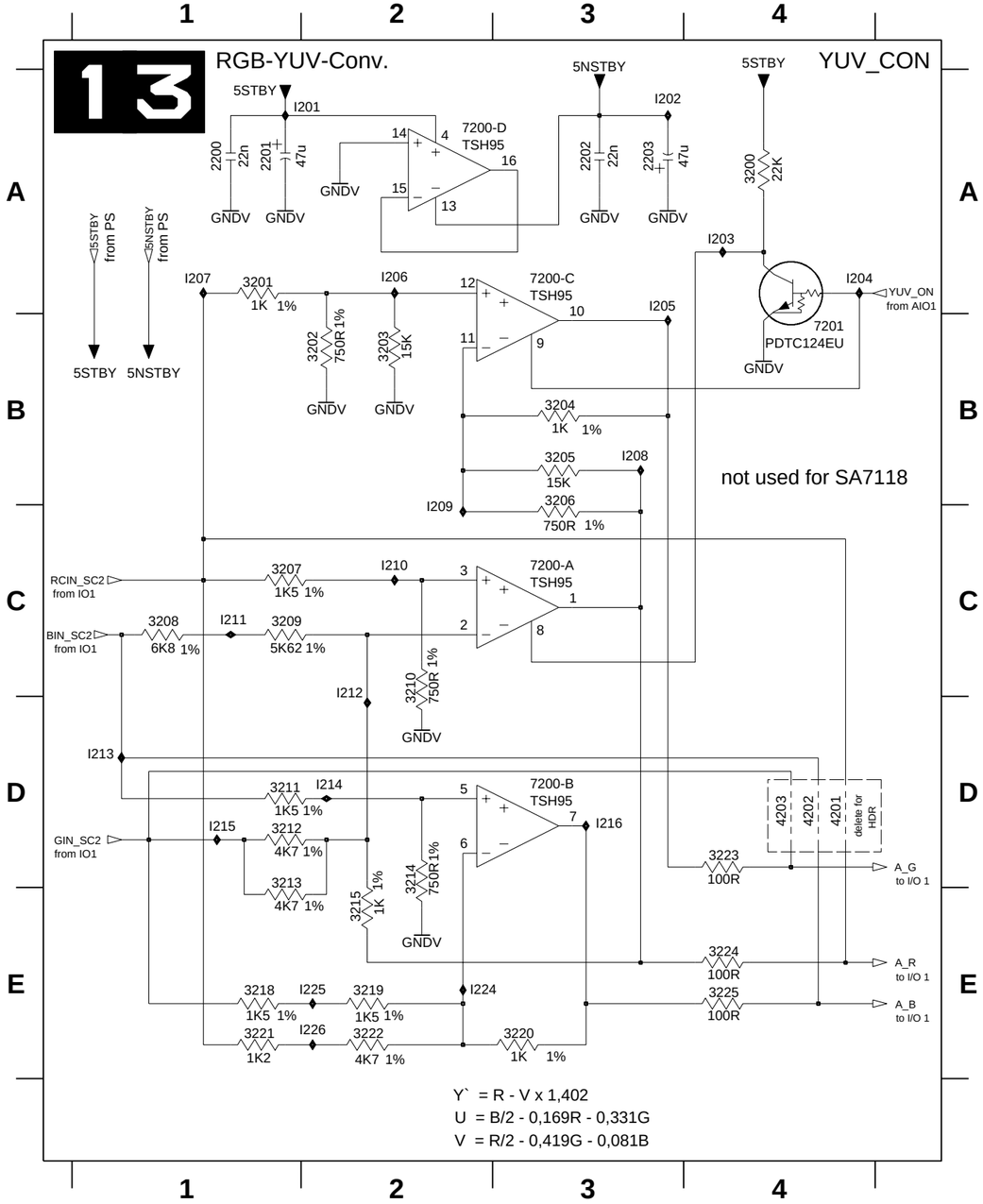
1900 B1	5002 B3
2000 A4	5003 B1
2001 E1	5004 B1
2002 C7	6000 A1
2003 C4	7000 A6
2004 C4	7001 A4
2005 D5	7002-A B8
2006 D5	7002-B E8
2007 D8	7004 E4
2008 D7	7005 C3
2009 D4	7007 A9
2010 E8	7008 B9
2011 E6	7009 A8
2012 E6	7010 B7
2013 E1	7011 A7
2014 E8	F0001 E1
2015 F1	F0002 E2
2016 F5	F0003 D2
2017 F6	F0005 D2
2018 F8	F0007 D2
2019 E5	F0009 D2
2020 F2	F0011 C2
2021 F2	F0012 C2
2022 E3	F0014 C2
2023 D3	F0016 C2
2024 A2	F0017 B1
2025 A3	F010 C9
2026 A3	F011 E9
2027 D3	F012 A1
2028 D3	F013 A1
2029 C3	F014 A1
2030 C3	I001 A1
3000 A2	I009 B6
3001 A6	I010 C6
3002 A6	I011 D6
3003 B4	I012 D6
3004 A3	I013 D5
3005 B7	I014 F6
3006 C7	I015 E3
3007 C7	I016 E3
3008 C6	I017 F3
3009 C8	I018 F3
3010 C6	I019 F3
3011 D7	I020 F3
3012 D7	I022 E8
3013 F2	I023 F5
3014 D2	I024 B8
3015 E2	I025 C8
3016 D2	I026 D8
3017 D7	I027 E8
3018 E6	I028 A4
3019 E6	I029 C4
3020 F2	I030 C5
3021 F2	I031 A6
3022 F8	I032 A6
3023 E3	I033 A4
3024 E3	I034 A4
3025 B2	I035 A4
3026 A2	I036 B4
3027 B2	I037 E3
3028 F5	I038 F1
3029 C8	I039 F1
3030 C3	
3032 F8	
3033 A8	
3034 A8	
3035 A7	
3036 B8	
3037 B7	
3038 B7	
3039 B9	
3040 B9	
3041 A9	
3042 A9	
3043 A6	
3044 A2	
5000 B3	
5001 E1	

■ SCHEMATIC DIAGRAM

A, B, G model

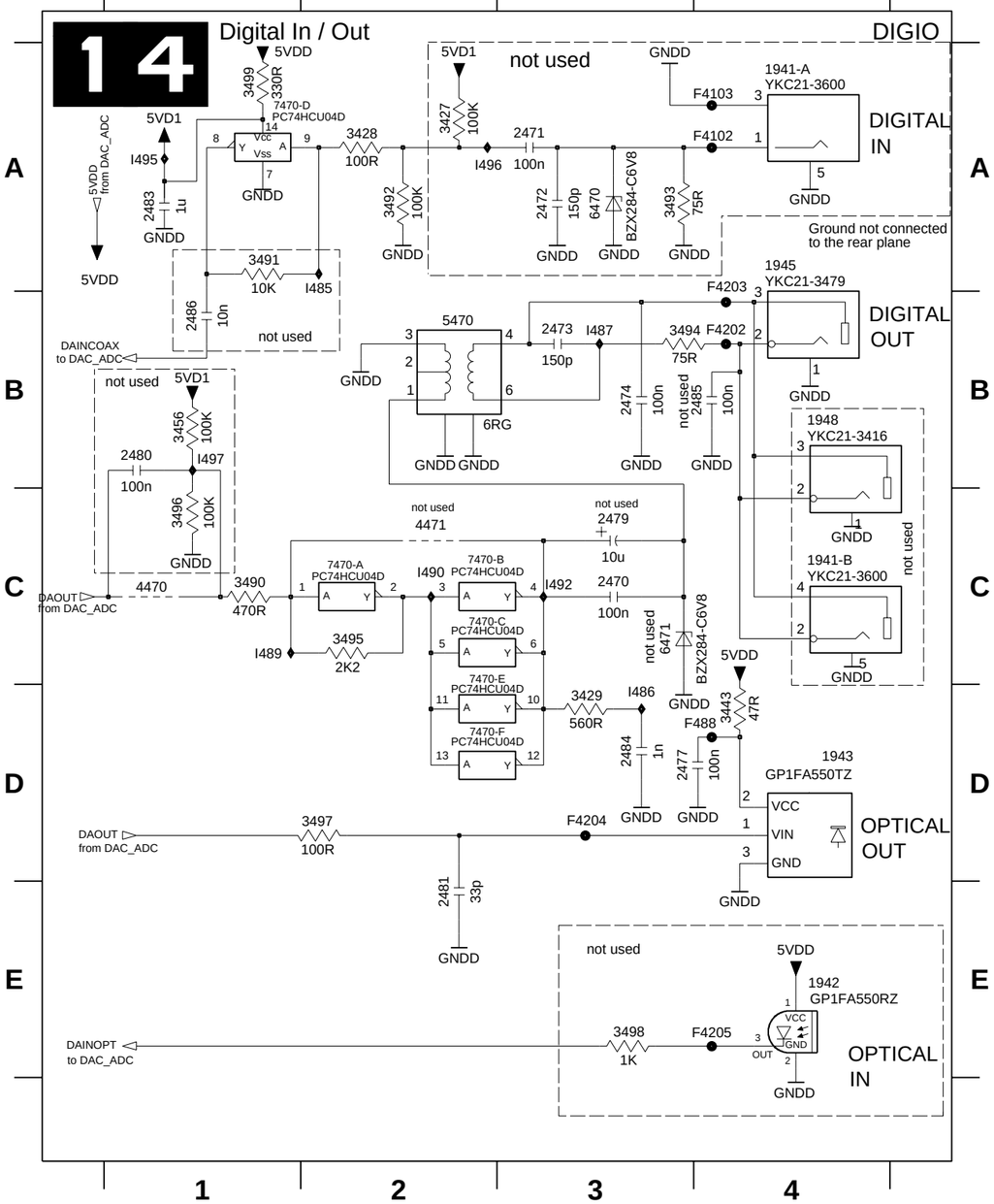
ANALOG: RGB-YUV-CONVERTER

2200 A1 2201 A1 2202 A3 2203 A3 3200 A4 3201 A1
3202 B2 3203 B2 3204 B3 3205 B3 3206 B3 3207 C1
3208 C1 3209 C1 3210 C2 3211 D1 3212 D1 3213 D1
3214 D2 3215 E2 3218 E1 3219 E2 3220 E3 3221 E1
3222 E2 3223 D4 3224 E4 3225 E4 4201 D4 4202 D4
4203 D4 7200-A C3 7200-B D3 7200-C A3 7200-D A2 7201 B4
I201 A2 I202 A3 I203 A4 I204 A5 I205 A3 I206 A2
I207 A1 I208 B3 I209 C2 I210 C2 I211 C1 I212 C2
I213 D1 I214 D2 I215 D1 I216 D3 I224 E2 I225 E2
I226 E2



ANALOG: DIGITAL IN / OUT

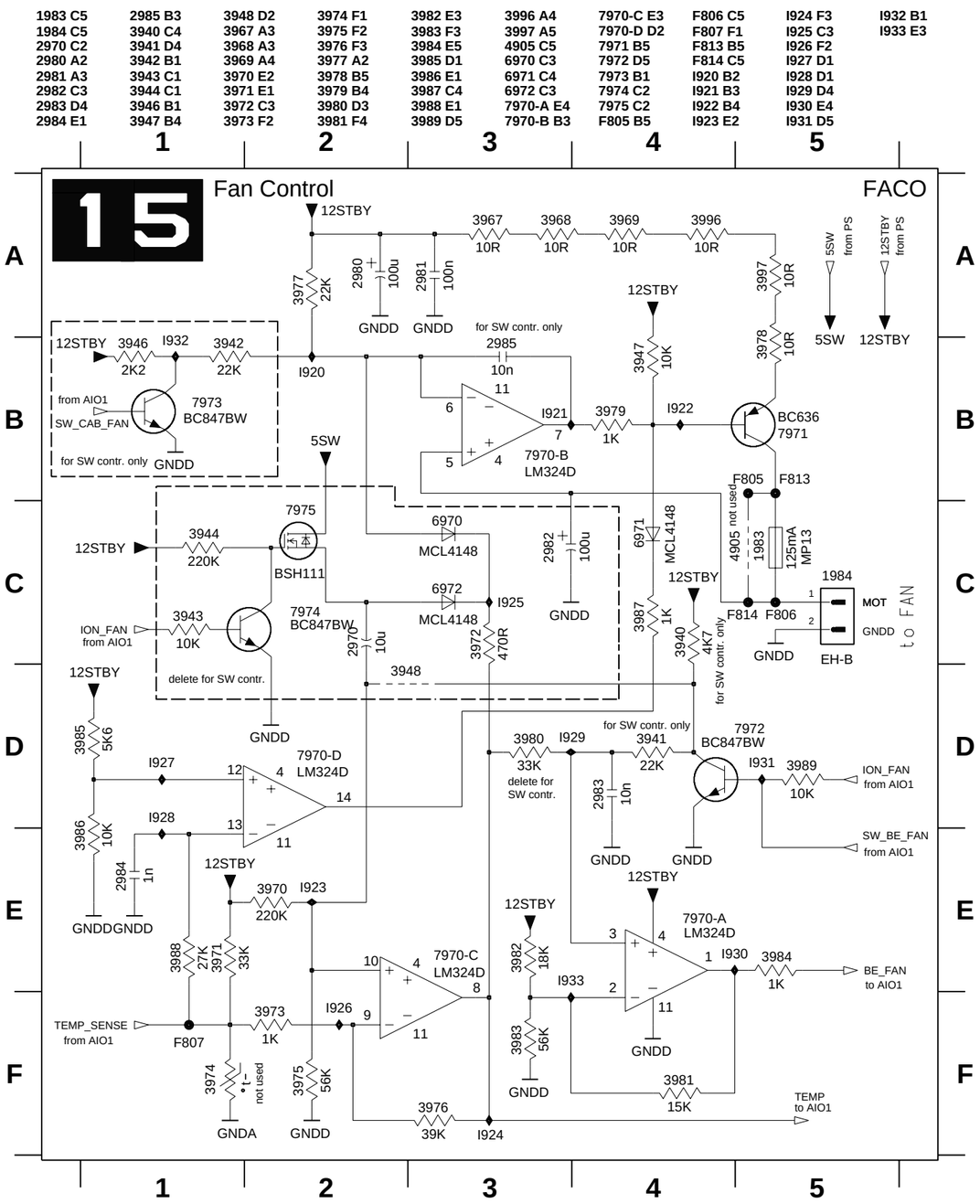
1941-A A4 1941-B C4 1942 E4 1943 D4 1945 A4 1948 B4 2470 C3
2471 A3 2472 A3 2473 B3 2474 B3 2477 D3 2479 C3 2480 B1
2481 E2 2483 A1 2484 D3 2485 B4 2486 B1 2487 A2 2488 A3
3429 D3 3443 D4 3456 B1 3490 C1 3491 A1 3492 A2 3493 A3
3494 B3 3495 C2 3496 C1 3497 D2 3498 E3 3499 A1 4470 C1
4471 C2 5470 B2 6470 A3 6471 C3 7470-A C2 7470-B C2 7470-C C2
7470-D A1 7470-E C2 7470-F D2 F4102 A4 F4103 A4 F4202 B4 F4203 A4
F4204 D3 F4205 E4 F488 D4 I485 A2 I486 A3 I489 A4 I490 A5
I491 A3 I492 A3 I495 A4 I496 A4 I497 B1



■ SCHEMATIC DIAGRAM

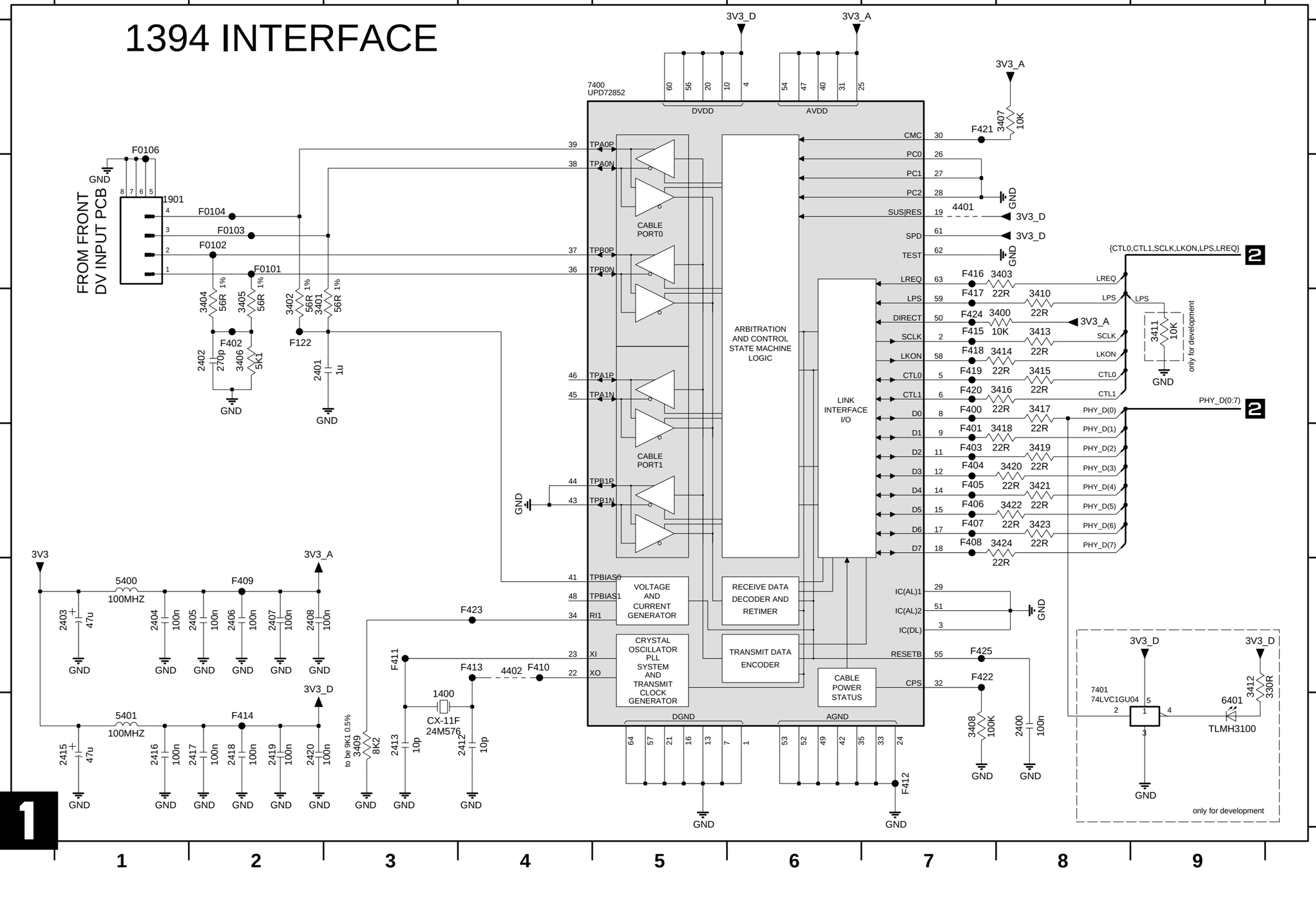
A, B, G model

ANALOG: FAN CONTROL



■ SCHEMATIC DIAGRAM

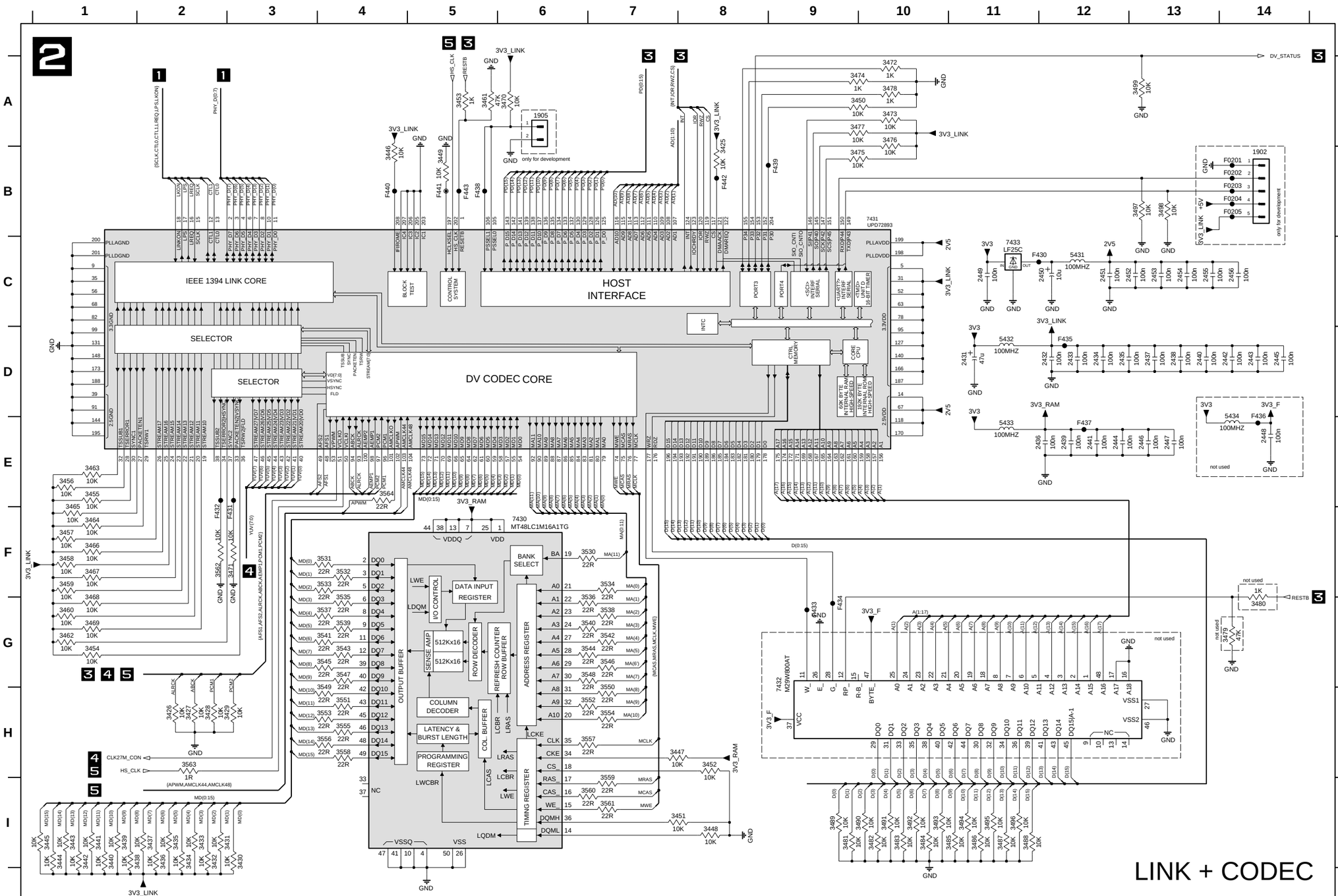
DVIO: 1394 INTERFACE



1400 F3
1901 B1
2400 F8
2401 C2
2402 C2
2403 E1
2404 E1
2405 E2
2406 E2
2407 E2
2408 E2
2412 F4
2413 F3
2415 F1
2416 F1
2417 F2
2418 F2
2419 F2
2420 F2
3400 C8
3401 C2
3402 C2
3403 B8
3404 C2
3405 C2
3406 C2
3407 A8
3408 F7
3409 F3
3410 C8
3411 C9
3412 E9
3413 C8
3414 C8
3415 C8
3416 C8
3417 C8
3418 D8
3419 D8
3420 D8
3421 D8
3422 D8
3423 D8
3424 D8
4401 B7
4402 E4
5400 E1
5401 F1
6401 F9
7400 A4
7401 E8
F0101 B2
F0102 B2
F0103 B2
F0104 B2
F0106 A1
F122 C2
F400 C7
F401 D7
F402 C2
F403 D7
F404 D7
F405 D7
F406 D7
F407 D7
F408 D7
F409 E2
F410 E4
F411 E3
F412 F7
F413 E4
F414 F2
F415 C7
F416 B7
F417 C7
F418 C7
F419 C7
F420 C7
F421 A7
F422 E7
F423 E4
F424 C7
F425 E7

■ SCHEMATIC DIAGRAM

DVIO: MICROPROCESSOR



1902 B14
1905 A6
2431 D11
2432 D12
2433 D12
2434 D12
2435 D12
2436 E12
2437 D13
2438 D13
2439 E12
2440 D13
2441 E12
2442 D14
2443 D14
2444 E12
2445 D14
2446 E13
2447 E13
2448 E14
2449 C11
2450 C12
2451 C12
2452 C13
2453 C13
2454 C13
2455 C13
2456 C14
3425 A8
3426 H2
3427 H2
3428 H2
3429 H3
3430 I3
3431 I2
3432 I2
3433 I2
3434 I2
3435 I2
3436 I2
3437 I2
3438 I1
3439 I1
3440 I1
3441 I1
3442 I1
3443 I1
3444 I1
3445 I1
3446 B4
3447 H7
3448 I8
3449 B5
3450 A9
3451 I8
3452 H8
3453 A5
3454 G1
3455 E1
3456 E1
3457 F1
3458 F1
3459 F1
3460 G1
3461 A5
3462 G1
3463 E1
3464 F1
3465 F1
3466 F1
3467 F1
3468 G1
3469 G1
3470 A6
3471 F3
3472 A10
3473 A10
3474 A9
3475 B9
3476 A10
3477 A9
3478 A10
3479 G14
3480 G14
3481 I9
3482 I10
3483 I10
3484 I10
3485 I11
3486 I11
3487 I11
3488 I11
3489 I9
3490 I10
3491 I10
3492 I10
3493 I10
3494 I11
3495 I11
3496 I11
3497 B13
3498 B13
3499 A13
3530 F7
3531 F4
3532 F4
3533 F4
3534 F7
3535 G4
3536 G7
3537 G4
3538 G7
3539 G4
3540 G7
3541 G4
3542 G7
3543 G4
3544 G7
3545 G4
3546 G7
3547 G4
3548 G7
3549 H4
3550 H7
3551 H4
3552 H7
3553 H4
3554 H7
3555 H4
3556 H4
3557 H7
3558 H4
3559 I7
3560 I7
3561 I7
3562 F2
3563 H2
3564 E4
5431 C12
5432 D11
5433 E11
5434 E14
7430 F6
7431 B10
7432 H9
7433 C11
F0201 B14
F0202 B14
F0203 B14
F0204 B14
F0205 B14
F430 C12
F431 F3
F432 F2
F433 G9
F434 G9
F435 D12
F436 E14
F437 E12
F438 B5
F439 B9
F440 B4
F441 B5
F442 B8
F443 B5

■ SCHEMATIC DIAGRAM

DVIO: FIFO & CONTROL

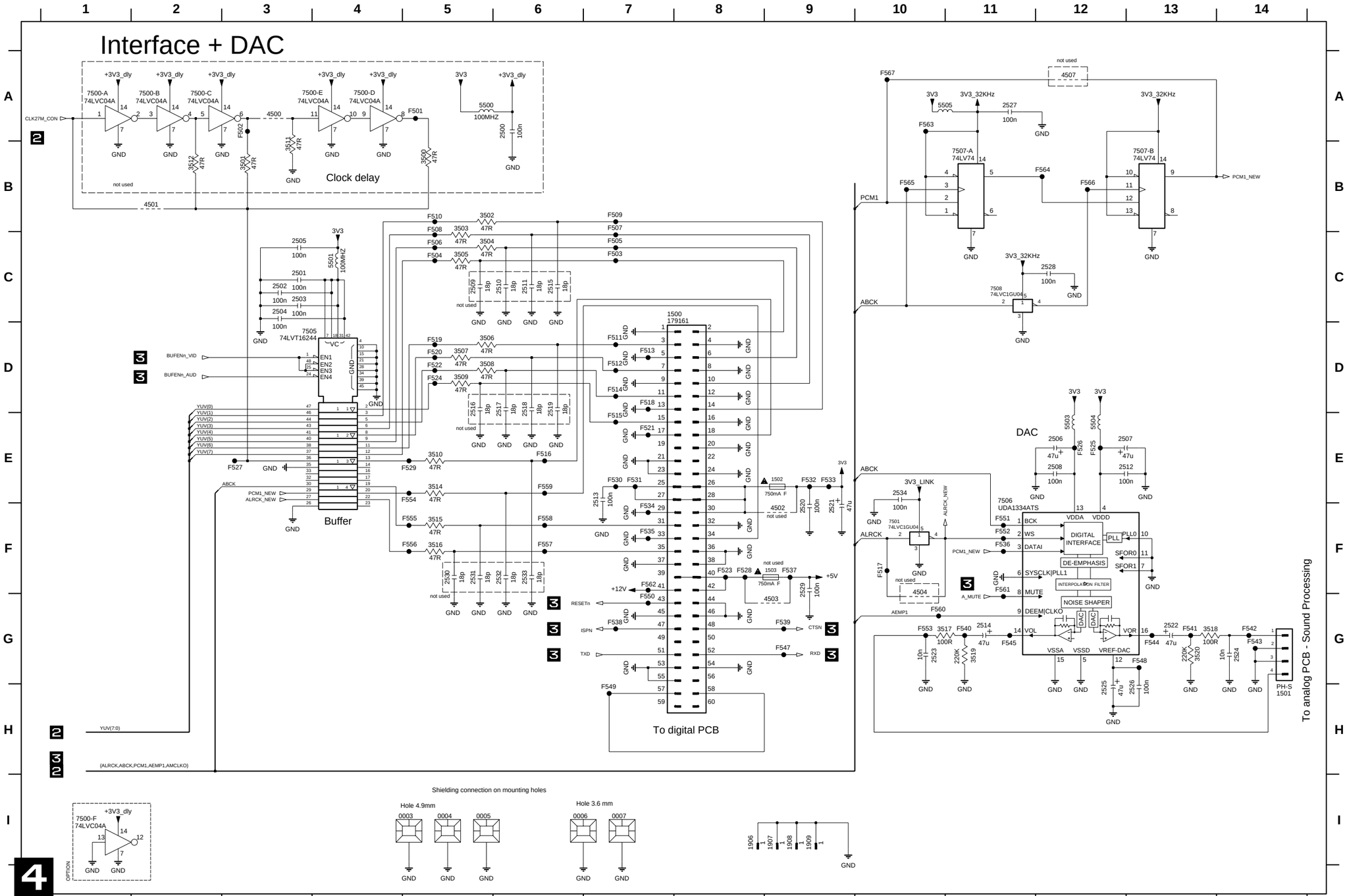
uP- Part

To front DV input PCB

1800 C6 F837 C2
1903 E13 F838 C2
1904 G12 F839 E2
2801 B6
2802 C6
2803 E13
2804 E13
2805 C2
2806 C5
2807 H11
2808 H12
2809 H12
2810 H13
2811 C1
2812 H13
2813 A2
2814 A5
2816 G3
2817 H3
2818 H3
2819 I2
2820 D5
2821 E6
2822 B2
3800 E11
3801 C1
3802 B5
3803 F4
3804 F2
3805 F2
3806 G2
3807 G2
3808 C7
3809 C5
3810 F2
3811 F3
3812 F3
3813 F3
3814 C2
3815 C3
3816 C3
3817 A3
3818 A5
3819 A4
3820 A2
3821 C2
3822 G2
3823 C3
3824 C3
3825 G3
3826 I2
3827 I3
3828 D5
3829 H2
3831 D4
3832 E4
3833 I6
3834 I6
3835 E3
3836 E2
3837 I3
3838 A2
3839 D2
5800 E12
5801 H12
5802 A1
6800 E12
6801 D3
6802 D3
6803 C1
6804 A6
7800 E11
7801 B4
7802 C8
7803 A4
7804 A4
7805 A3
7806 C4
7807 G2
7808 H2
7809 D5
7810 B2
7811 E1
F0301 E13
F0302 E13
F0401 G12
F0402 G13
F0403 G12
F0404 G13
F0405 G12
F0406 G13
F800 B7
F801 C7
F802 E11
F803 E10
F804 G4
F805 B8
F806 I4
F808 C7
F809 D7
F810 D7
F811 C7
F812 G8
F815 H6
F816 H6
F817 E7
F818 E7
F819 C7
F820 E7
F822 F4
F823 F4
F824 F4
F825 G4
F826 G4
F827 A3
F829 A5
F830 A2
F831 D2
F832 C3
F833 C3
F834 D3
F835 C4
F836 A5

■ SCHEMATIC DIAGRAM

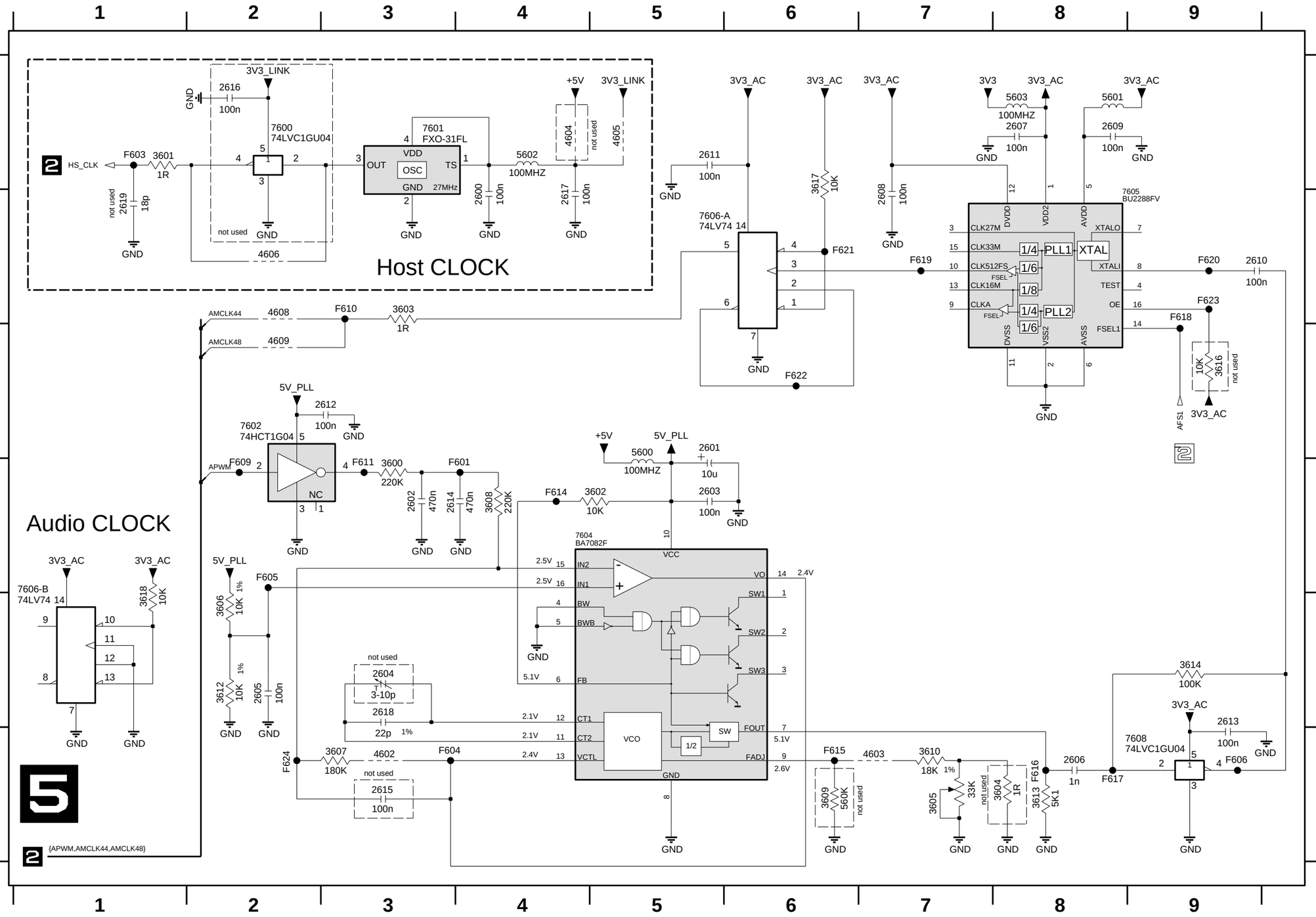
DVIO: DVCODEC



0003 I4
0004 I5
0005 I5
0006 I6
0007 I7
1500 C7
1501 H14
1502 E9
1503 F9
1906 I8
1907 I9
1908 I9
1909 I9
2500 A6
2501 C3
2502 C3
2503 C3
2504 C3
2505 C3
2506 E12
2507 E12
2508 E12
2509 C5
2510 C6
2511 C6
2512 E12
2513 E7
2514 G11
2515 C6
2516 D5
2517 D6
2518 D6
2519 D6
2520 F9
2521 F9
2522 G13
2523 G10
2524 G14
2525 H12
2526 H13
2527 A11
2528 C12
2529 F9
2530 F5
2531 F5
2532 F6
2533 F6
2534 E10
3500 B5
3501 B3
3502 B5
3503 B5
3504 C5
3505 C5
3506 D5
3507 D5
3508 D5
3509 D5
3510 E5
3511 B3
3512 B2
3514 E5
3515 F5
3516 F5
3517 G10
3518 G13
3519 G11
3520 G13
4500 A3
4501 B2
4502 F9
4503 G9
4504 G10
4507 A12
5500 A5
5501 C4
5503 E12
5504 E12
5505 A10
7500-A A1
7500-B A2
7500-C A2
7500-D A4
7500-E A3
7500-F I1
7501 F10
7505 D4
7506 E11
7507-A B11
7507-B B13
7508 C11
F501 A5
F502 A3
F503 C7
F504 C5
F505 C7
F506 C5
F507 B7
F508 B5
F509 B7
F510 B5
F511 D7
F512 D7
F513 D7
F514 D7
F515 E7
F516 E6
F517 F10
F518 D7
F519 D5
F520 D5
F521 E7
F522 D5
F523 F8
F524 D5
F525 E12
F526 E12
F527 E3
F528 E8
F529 E5
F530 E7
F531 E7
F532 E9
F533 E9
F534 F7
F535 F7
F536 F11
F537 F9
F538 G7
F539 G9
F540 G11
F541 G13
F542 G14
F543 G14
F544 G13
F545 G11
F547 G9
F548 G13
F549 H7
F550 G7
F551 F11
F552 F11
F553 G10
F554 E5
F555 F5
F556 F5
F557 F6
F558 F6
F559 E6
F560 G10
F561 F11
F562 F7
F563 A10
F564 B12
F565 B10
F566 B12
F567 A10

■ SCHEMATIC DIAGRAM

DVIO: AUDIO & VIDEO OUTPUT

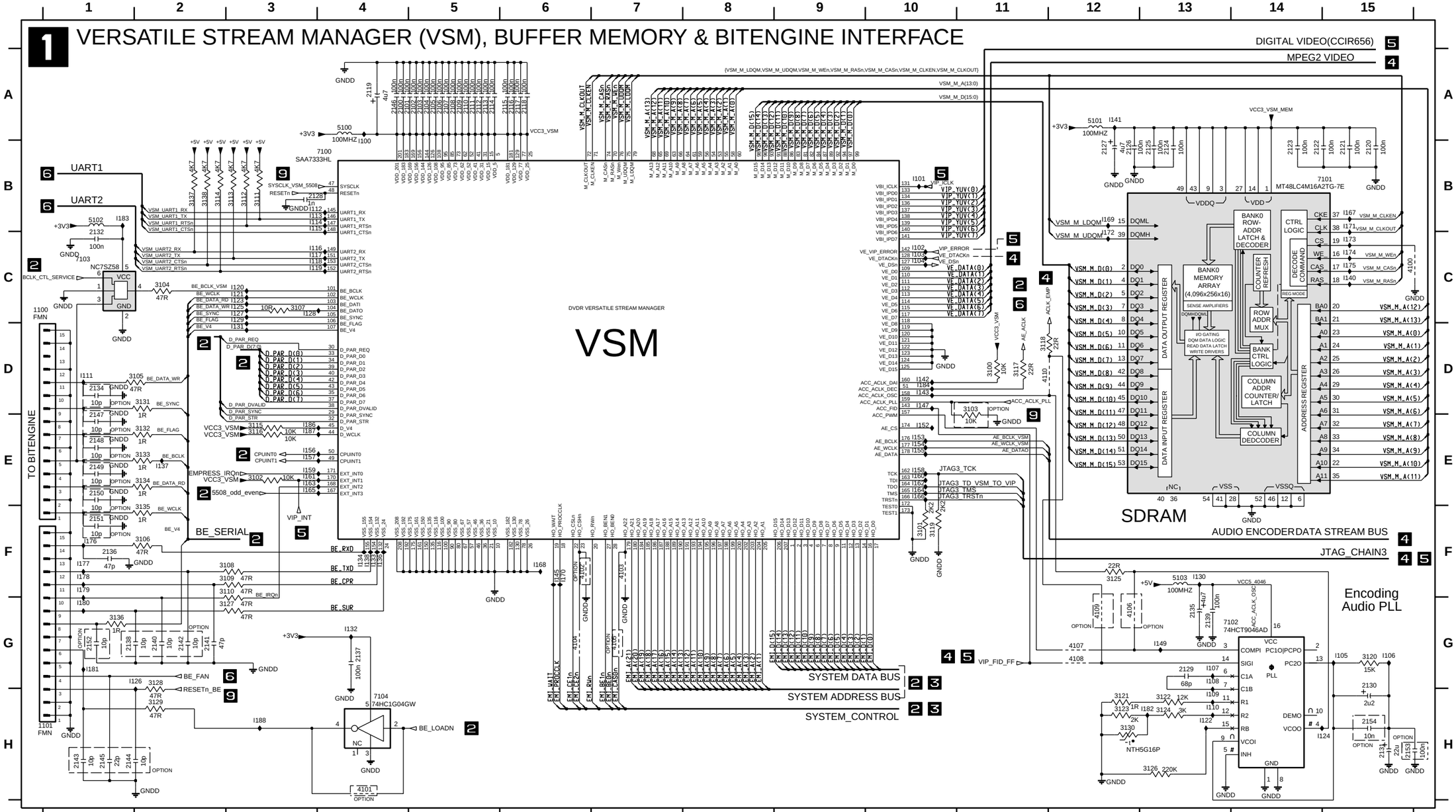


2600 B4
2601 C5
2602 D3
2603 D5
2604 E3
2605 E2
2606 F8
2607 A8
2608 B7
2609 A8
2610 B9
2611 A5
2612 C3
2613 E9
2614 D3
2615 F3
2616 A2
2617 B4
2618 E3
2619 B1
3600 D3
3601 A1
3602 D5
3603 B3
3604 F8
3605 F7
3606 E2
3607 F3
3608 D4
3609 F6
3610 F7
3612 E2
3613 F8
3614 E9
3616 C9
3617 A6
3618 E1
4602 F3
4603 F7
4604 A4
4605 A5
4606 B2
4608 B2
4609 C2
5600 C5
5601 A8
5602 A4
5603 A8
7600 A2
7601 A3
7602 C2
7604 D4
7605 B8
7606-A B5
7606-B D1
7608 F8
F601 D4
F603 A1
F604 F3
F605 D2
F606 F9
F609 D2
F610 B3
F611 D3
F614 D4
F615 F6
F616 F8
F617 F8
F618 B9
F619 B7
F620 B9
F621 B6
F622 C6
F623 B9
F624 F2

■ SCHEMATIC DIAGRAM

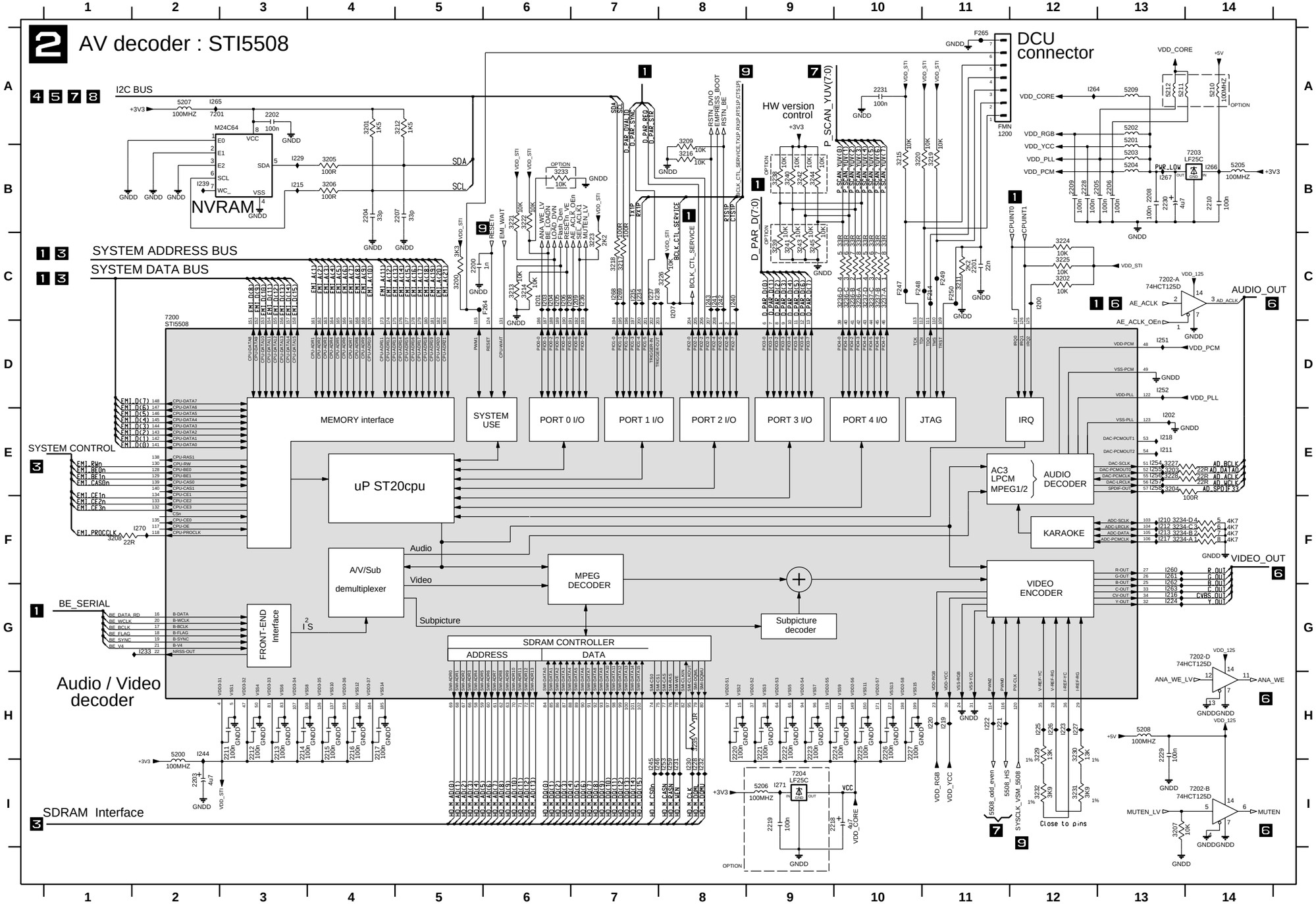
DIGITAL: VSM, BUFFER MEMORY AND BIT ENGINE INTERFACE

1100	C1	2106	A5	2114	A5	2122	B14	2130	G15	2139	G13	2147	D1	3102	E3	3110	F3	3118	D11	3126	H12	3134	E2	4103	F7	7101	B14
1101	H1	2107	A5	2115	A6	2123	B14	2131	H15	2140	G2	2148	E1	3103	D11	3111	B3	3119	F10	3127	G3	3135	E2	4104	G6	7102	G13
2100	A4	2108	A5	2116	A6	2124	B13	2132	B1	2141	G2	2149	E1	3104	C2	3112	B3	3120	G15	3128	G2	3136	G1	4105	G7	7103	C1
2101	A5	2109	A5	2117	A6	2125	B13	2134	D1	2142	G2	2150	E1	3105	D2	3113	B3	3121	G12	3129	H2	3137	B2	5100	A4	7104	H4
2102	A5	2110	A5	2118	A6	2126	B12	2135	G13	2143	H1	2151	F1	3106	F2	3114	B2	3122	H12	3130	H12	3138	B2	5101	A12		
2103	A5	2111	A5	2119	A4	2127	B12	2136	F1	2144	H1	2152	G1	3107	C3	3115	E3	3123	H12	3131	D2	4100	C15	5102	B1		
2104	A5	2112	A5	2120	B15	2128	B3	2137	G4	2145	H1	3100	D11	3108	F3	3116	E3	3124	H12	3132	E2	4101	H4	5103	F13		
2105	A5	2113	A5	2121	B15	2129	G13	2138	G1	2146	A4	3101	F10	3109	F3	3117	D11	3125	G14	3133	E2	4102	F6	7100	B4		



■ SCHEMATIC DIAGRAM

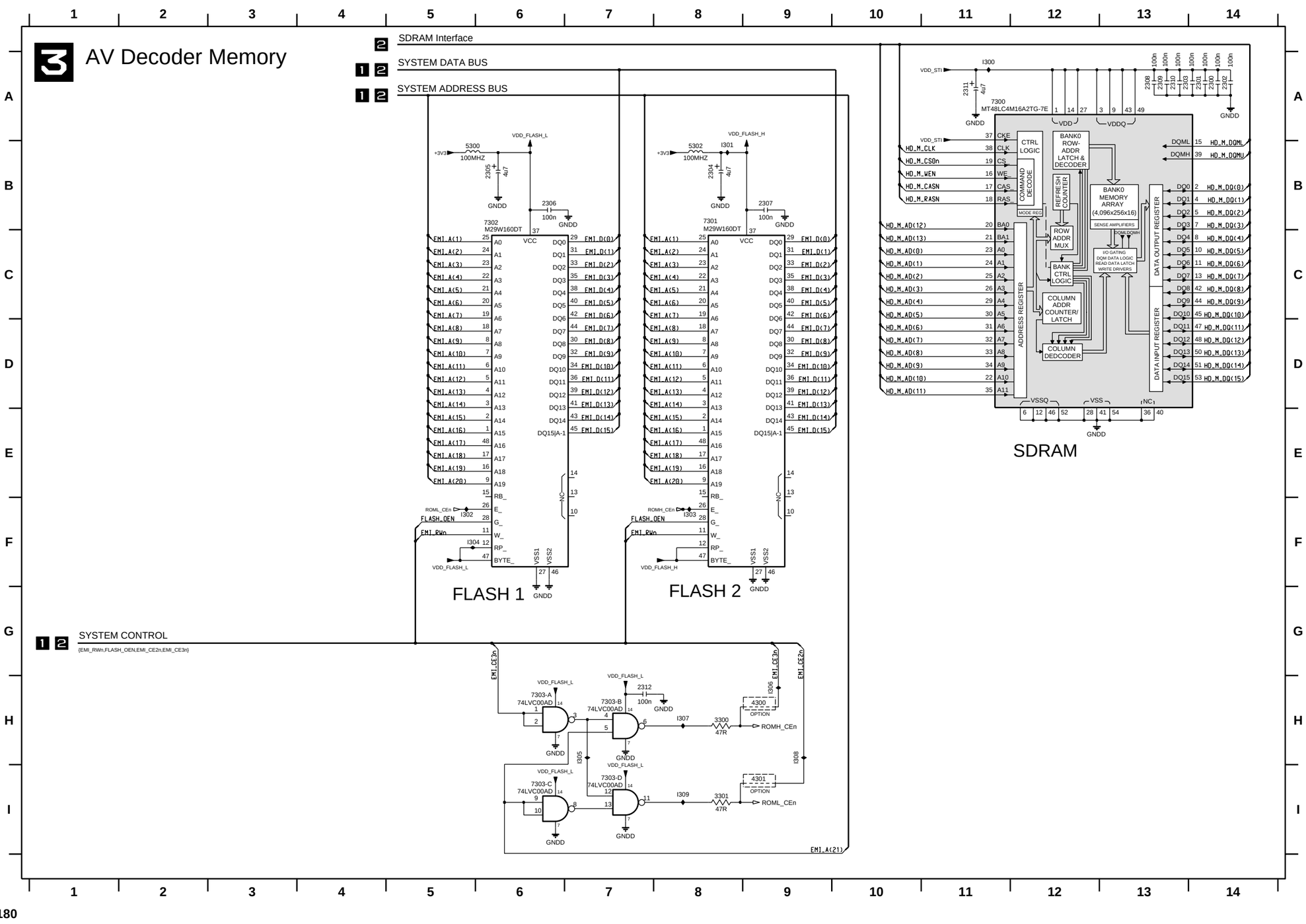
DIGITAL: AV DECODER STI5508



1200	A11	5207	A2
2200	C5	5208	H13
2201	C11	5209	A13
2202	A3	5210	A14
2203	I2	5211	A13
2204	B4	5212	A13
2205	B13	7200	C2
2206	B13	7201	A2
2207	B5	7202-A	C13
2208	B13	7202-B	I14
2209	B12	7202-D	G14
2210	B14	7203	B14
2211	H3	7204	I9
2212	H3	F214	C11
2213	H3	F247	C10
2214	H3	F248	C10
2215	H4	F249	C11
2216	H4	F250	C11
2217	H4	F264	C6
2218	I10	F265	A11
2219	I9		
2220	H8		
2221	H9		
2222	H9		
2223	H9		
2224	H10		
2225	H10		
2226	H10		
2227	H10		
2228	B12		
2229	H13		
2230	B13		
2231	A10		
3200	C5		
3201	A4		
3202	C12		
3203	E13		
3204	E13		
3205	B4		
3206	B4		
3207	I13		
3208	F1		
3209	A8		
3211	C11		
3212	A5		
3213	C6		
3214	C6		
3215	B10		
3216	B8		
3217	C7		
3218	C7		
3219	B11		
3220	B10		
3221	B6		
3222	B6		
3223	C7		
3224	C12		
3225	C12		
3226	C8		
3227	E13		
3228	E13		
3229	H12		
3230	H12		
3231	I12		
3232	I12		
3233	B6		
3234-A	F13		
3234-B	F13		
3234-C	F13		
3234-D	F13		
3235	H8		
3236-A	C10		
3236-B	C10		
3236-C	C10		
3236-D	C10		
3237-A	C10		
3237-B	C10		
3237-C	C10		
3237-D	C10		
3238	B9		
3239	C9		
3240	B9		
3241	C9		
3242	B9		
3243	C9		
3244	B9		
3245	C9		
5200	H2		
5201	A13		
5202	A13		
5203	B13		
5204	B13		
5205	B14		
5206	I9		

■ SCHEMATIC DIAGRAM

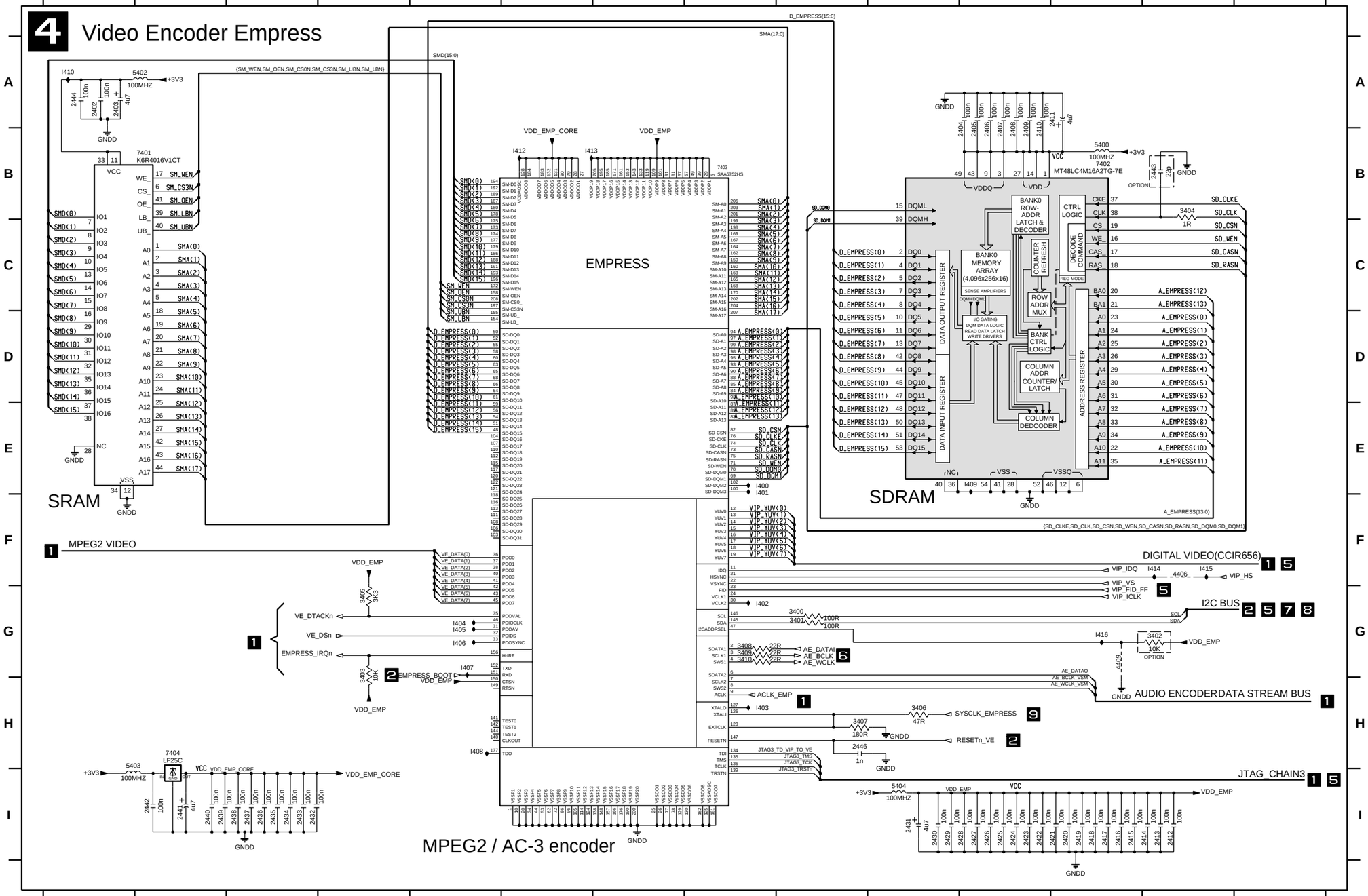
DIGITAL: AV DECODER MEMORY



2300	A14
2301	A14
2302	A14
2303	A13
2304	B8
2305	B6
2306	B6
2307	B9
2308	A13
2309	A13
2310	A13
2311	A11
2312	H7
3300	H8
3301	I8
4300	H9
4301	I9
5300	B5
5302	B8
7300	A11
7301	B8
7302	B6
7303-A	H6
7303-B	H7
7303-C	I6
7303-D	I7

■ SCHEMATIC DIAGRAM

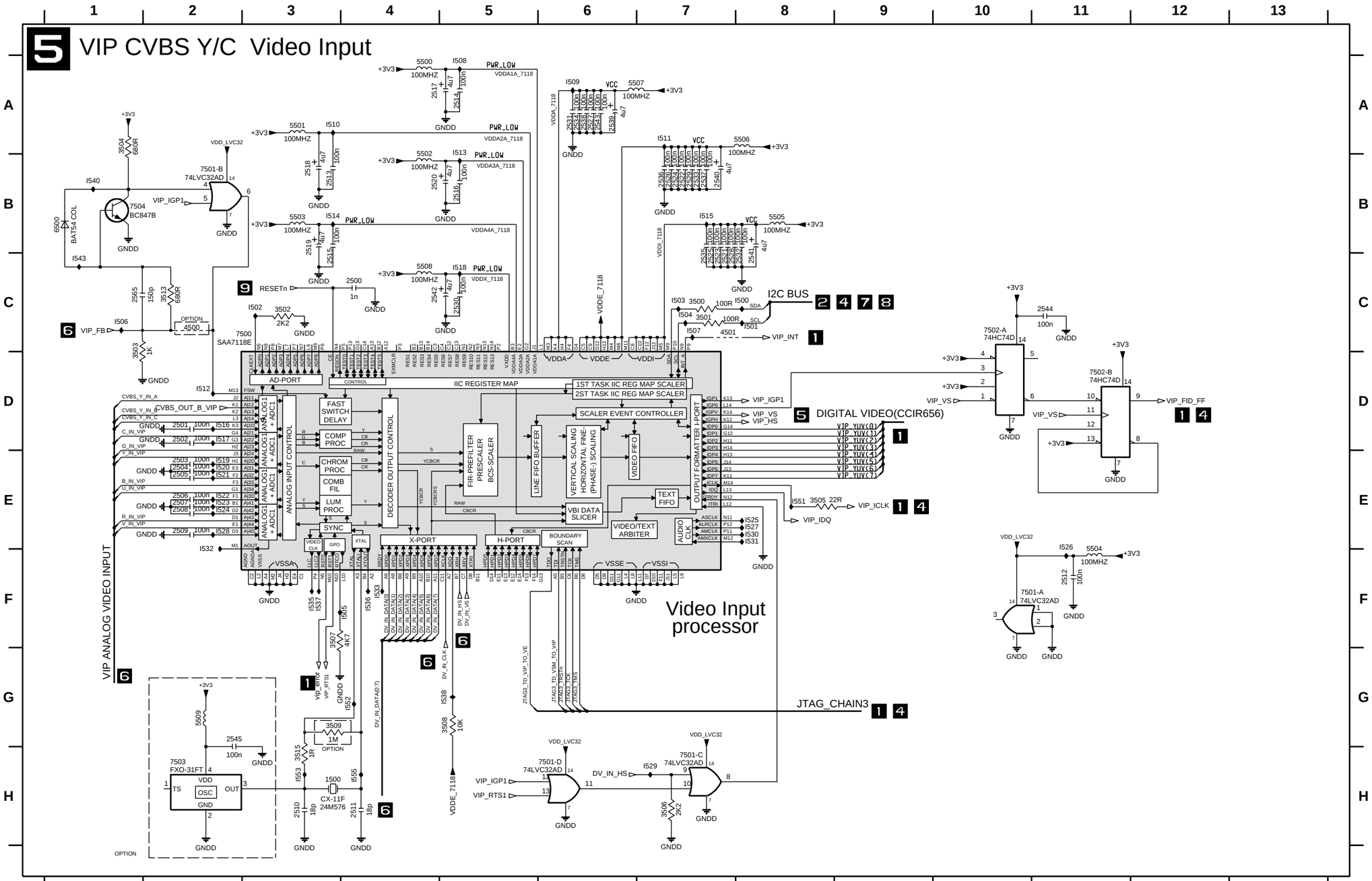
DIGITAL: VIDEO ENCODER, EMPRESS



2402	A1
2403	A1
2404	B11
2405	B11
2406	B11
2407	B11
2408	B11
2409	B11
2410	B11
2411	A12
2412	I13
2413	I13
2414	I13
2415	I12
2416	I12
2417	I12
2418	I12
2419	I12
2420	I12
2421	I12
2422	I11
2423	I11
2424	I11
2425	I11
2426	I11
2427	I11
2428	I11
2429	I10
2430	I10
2431	I10
2432	I3
2433	I3
2434	I3
2435	I3
2436	I3
2437	I3
2438	I3
2439	I2
2440	I2
2441	I2
2442	I2
2443	B13
2444	A1
2446	H9
3400	G9
3401	G9
3402	G13
3403	G4
3404	B13
3405	G4
3406	H10
3407	H9
3408	G8
3409	G8
3410	G8
4406	F13
4409	G12
5400	B12
5402	A2
5403	H1
5404	I10
7401	B2
7402	B12
7403	B8
7404	H2

■ SCHEMATIC DIAGRAM

DIGITAL: VIP CVBS Y/C VIDEO INPUT



1500	H3
2500	C4
2501	D2
2502	D2
2503	E2
2504	E2
2505	E2
2506	E2
2507	E2
2508	E2
2509	E2
2510	H3
2511	H4
2512	F11
2513	B3
2514	A5
2515	C3
2516	B5
2517	A4
2518	B3
2519	B3
2520	B4
2521	C7
2522	B7
2523	C7
2524	B7
2525	C7
2526	B7
2527	A6
2528	C7
2529	B7
2530	C5
2531	A6
2532	C8
2533	B7
2534	A6
2535	C7
2536	B7
2537	B7
2538	A6
2539	A6
2540	B7
2541	B8
2542	C4
2543	A6
2544	C11
2545	G2
2565	C1
3500	C7
3501	C7
3502	C3
3503	C1
3504	A1
3505	E8
3506	H7
3507	F3
3508	G5
3509	G3
3513	C2
3515	H3
4500	C2
4501	C7
5500	A4
5501	A3
5502	A4
5503	B3
5504	E11
5505	B8
5506	A8
5507	A6
5508	C4
5509	G2
6500	B1
7500	C3
7501-A	F11
7501-B	B2
7501-C	H7
7501-D	H6
7502-A	C10
7502-B	D11
7503	H2
7504	B1

■ SCHEMATIC DIAGRAM

DIGITAL: ANALOG P.C.B. CONS. VIDEO IN / OUTPUT

6 Analog P.C.B. Cons. Video In / Output

5 VIP ANALOG VIDEO INPUT

1 4 AUDIO ENCODER DATA STREAM BUS

2 AUDIO OUT

2 VIDEO_OUT

5 DV_IN_DATA(0:7)

1603 DIVIO 84816

1 UART2

9 UART1 1600 FMN

ANALOG BOARD INTERFACE AUDIO IN/OUT

ANALOG BOARD INTERFACE VIDEO IN/OUT

ANALOG BOARD INTERFACE CONTROL

1600	H14	7202-C	D12	2631	C12	3612	B2
1601	D14	7600	E6	2632	A2	3613	B9
1602	C14	7601	G10	2633	B9	3614	B2
1603	E2	7602	B3	2634	B2	3615	C9
2600	E6	7603	G6	2635	C9	3619	H9
2601	E5	7604	I10	2636	H9	3600	D13
2602	E5	7605	I6	3600	D13	3601	E5
2603	C12	7606	E10	3601	E5	3602	E6
2604	C13			3602	E6	3603	F6
2605	E10			3603	F6	3604	B12
2606	E9			3604	B12	3605	A10
2607	E9			3605	A10	3606	E8
2608	A6			3606	E8	3607	E9
2609	A6			3607	E9	3608	F10
2610	G6			3608	F10	3609	A9
2611	G5			3609	A9	3610	C10
2612	G5			3610	C10	3611	G5
2613	A9			3611	G5	3612	G6
2614	B9			3612	G6	3613	H6
2615	F10			3613	H6	3614	C9
2616	G9			3614	C9	3615	B3
2617	G9			3615	B3	3616	G8
2618	A9			3616	G8	3617	G9
2619	C9			3617	G9	3618	G10
2620	H6			3618	G10	3619	B2
2621	I5			3619	B2	3620	F1
2622	I5			3620	F1	3621	I5
2623	C12			3621	I5	3622	I6
2624	C12			3622	I6	3623	A12
2625	H10			3623	A12	3624	I6
2626	I9			3624	I6	3625	A12
2627	I9			3625	A12	3626	I8
2628	C6			3626	I8	3627	I9
2629	A6			3627	I9	3628	I10
2630	A2			3628	I10	3629	A6
2631	C12			3629	A6	3630	C6
2632	A2			3630	C6	3631	B10
2633	B9			3631	B10	3632	B6
2634	B2			3632	B6	3633	C6
2635	C9			3633	C6	3634	B9
2636	H9			3634	B9	3635	B12
3600	D13			3635	B12	3636	B2
3601	E5			3636	B2	3637	B12
3602	E6			3637	B12	3638	B3
3603	F6			3638	B3	4600	G3
3604	B12			3639	G3	4601	G1
3605	A10			3640	G1	4602	G3
3606	E8			3641	G3	5600	E5
3607	E9			3642	E5	5601	G9
3608	F10			3643	G9	5602	I5
3609	A9			3644	I5	5603	G5
3610	C10			3645	G5	5604	I9
3611	G5			3646	I9	5605	E9
3612	G6			3647	I9	5606	A2
3613	H6			3648	I9	5607	H9
3614	C9			3649	I9		
3615	B3			3650	I9		
3619	H9			3651	I9		
3600	D13			3652	I9		
3601	E5			3653	I9		
3602	E6			3654	I9		
3603	F6			3655	I9		
3604	B12			3656	I9		
3605	A10			3657	I9		
3606	E8			3658	I9		
3607	E9			3659	I9		
3608	F10			3660	I9		
3609	A9			3661	I9		
3610	C10			3662	I9		
3611	G5			3663	I9		
3612	G6			3664	I9		
3613	H6			3665	I9		
3614	C9			3666	I9		
3615	B3			3667	I9		
3619	H9			3668	I9		
3600	D13			3669	I9		
3601	E5			3670	I9		
3602	E6			3671	I9		
3603	F6			3672	I9		
3604	B12			3673	I9		
3605	A10			3674	I9		
3606	E8			3675	I9		
3607	E9			3676	I9		
3608	F10			3677	I9		
3609	A9			3678	I9		
3610	C10			3679	I9		
3611	G5			3680	I9		
3612	G6			3681	I9		
3613	H6			3682	I9		
3614	C9			3683	I9		
3615	B3			3684	I9		
3619	H9			3685	I9		
3600	D13			3686	I9		
3601	E5			3687	I9		
3602	E6			3688	I9		
3603	F6			3689	I9		
3604	B12			3690	I9		
3605	A10			3691	I9		
3606	E8			3692	I9		
3607	E9			3693	I9		
3608	F10			3694	I9		
3609	A9			3695	I9		
3610	C10			3696	I9		
3611	G5			3697	I9		
3612	G6			3698	I9		
3613	H6			3699	I9		
3614	C9			3700	I9		
3615	B3			3701	I9		
3619	H9			3702	I9		
3600	D13			3703	I9		
3601	E5			3704	I9		
3602	E6			3705	I9		
3603	F6			3706	I9		
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3605	A10			3708	I9		
3606	E8			3709	I9		
3607	E9			3710	I9		
3608	F10			3711	I9		
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3610	C10			3713	I9		
3611	G5			3714	I9		
3612	G6			3715	I9		
3613	H6			3716	I9		
3614	C9			3717	I9		
3615	B3			3718	I9		
3619	H9			3719	I9		
3600	D13			3720	I9		
3601	E5			3721	I9		
3602	E6			3722	I9		
3603	F6			3723	I9		
3604	B12			3724	I9		
3605	A10			3725	I9		
3606	E8			3726	I9		
3607	E9			3727	I9		
3608	F10			3728	I9		
3609	A9			3729	I9		
3610	C10			3730	I9		
3611	G5			3731	I9		
3612	G6			3732	I9		
3613	H6			3733	I9		
3614	C9			3734	I9		
3615	B3			3735	I9		
3619	H9			3736	I9		
3600	D13			3737	I9		
3601	E5			3738	I9		
3602	E6			3739	I9		
3603	F6			3740	I9		
3604	B12			3741	I9		
3605	A10			3742	I9		
3606	E8			3743	I9		
3607	E9			3744	I9		
3608	F10			3745	I9		
3609	A9			3746	I9		
3610	C10			3747	I9		
3611	G5			3748	I9		
3612	G6			3749	I9		
3613	H6			3750	I9		
3614	C9			3751	I9		
3615	B3			3752	I9		
3619	H9			3753	I9		
3600	D13			3754	I9		
3601	E5			3755	I9		
3602	E6			3756	I9		
3603	F6			3757	I9		
3604	B12			3758	I9		
3605	A10			3759	I9		
3606	E8			3760	I9		
3607	E9			3761	I9		
3608	F10			3762	I9		
3609	A9			3763	I9		
3610	C10			3764	I9		
3611	G5			3765	I9		
3612	G6			3766	I9		
3613	H6			3767	I9		
3614	C9			3768	I9		
3615	B3			3769	I9		
3619	H9			3770	I9		
3600	D13			3771	I9		
3601	E5			3772	I9		
3602	E6			3773	I9		
3603	F6			3774	I9		
3604	B12			3775	I9		
3605	A10			3776	I9		
3606	E8			3777	I9		
3607	E9			3778	I9		
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3609	A9			3780	I9		
3610	C10			3781	I9		
3611	G5			3782	I9		
3612	G6			3783	I9		
3613	H6			3784	I9		
3614	C9			3785	I9		
3615	B3			3786	I9		
3619	H9			3787	I9		
3600	D13			3788	I9		
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3602	E6			3790	I9		
3603	F6			3791	I9		
3604	B12			3792	I9		
3605	A10			3793	I9		
3606	E8			3794	I9		
3607	E9			3795	I9		
3608	F10			3796	I9		
3609	A9			3797	I9		
3610	C10			3798	I9		
3611	G5			3799	I9		
3612	G6			3800	I9		
3613	H6			3801	I9		
3614	C9			3802	I9		
3615	B3			3803	I9		
3619	H9			3804	I9		
3600	D13			3805	I9		
3601	E5			3806	I9		
3602	E6			3807	I9		
3603	F6			3808	I9		
3604	B12			3809	I9		
3605	A10			3810	I9		
3606	E8			3811	I9		
3607	E9			3812	I9		
3608	F10			3813	I9		
3609	A9			3814	I9		
3610	C10			3815	I9		
3611	G5			3816	I9		
3612	G6			3817	I9		
3613	H6			3818	I9		
3614	C9			3819	I9		
3615	B3			3820	I9		
3619	H9			3821	I9		
3600	D13			3822	I9		
3601	E5			3823	I9		
3602	E6			3824	I9		
3603	F6			3825	I9		
3604	B12			3826	I9		
3605	A10			3827	I9		
3606	E8			3828	I9		
3607	E9			3829	I9		
3608	F10			3830	I9		
3609	A9			3831	I9		
3610	C10			3832	I9		
3611	G5			3833	I9		
3612	G6			3834	I9		
3613	H6			3835	I9		
3614	C9			3836	I9		
3615	B3			3837	I9		
3619	H9			3838	I9		
3600	D13			3839	I9		
3601	E5			3840	I9		
3602	E6			3841	I9		
3603	F6			3842	I9		
3604	B12			3843	I9		
3605	A10			3844	I9		
3606	E8			3845	I9		
3607	E9			3846	I9		
3608	F10			3847	I9		
3609	A9			3848	I9		
3610	C10			3849	I9		
3611	G5			3850	I9		
3612	G6			3851	I9		
3613	H6			3852	I9		
3614	C9			3853	I9		
3615	B3			3854	I9		
3619	H9			3855	I9		
3600	D13			3856	I9		
3601	E5			3857	I9		
3602	E6			3858	I9		
3603	F6			3859	I9		
3604	B12			3860	I9		
3605	A10			3861	I9		
3606	E8			3862	I9		
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3608	F10			3864	I9		
3609	A9			3865	I9		
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3611	G5			3867	I9		
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3600	D13			3873	I9		
3601	E5			3874	I9		
3602	E6			3875	I9		
3603	F6			3876	I9		
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3607	E9			3897	I9		
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3609	A9			3899	I9		
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3611	G5			3901	I9		
3612	G6			3902	I9		
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3603	F6			3910	I9		
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3600	D13			3924	I9		
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3614	C9			4006	I9		
3615	B3			4007	I9		
3619	H9			4008	I9		
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3603	F6			4012	I9		
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3612	G6			4021	I9		
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3613	H6			4124	I9		
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3619	H9			4144	I9		
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3609	A9			4154	I9		
3610	C10			4155	I9		
3611	G5			4156	I9		
3612	G6			4157	I9		
3613	H6			4158	I9		
3614	C9			4159	I9		
3615	B3			4160	I9		
3619	H9			4161	I9		
3600	D13			4162	I9		
3601	E5			4163	I9		
3602	E6			4164	I9		
3603	F6			4165	I9		
3604	B12			4166	I9		
3605	A10			4167	I9		
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3607	E9			4169	I9		
3608	F10			4170	I9		
3609	A9			4171	I9		
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3611	G5			4173	I9		
3612	G6			4174	I9		
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3614	C9			4176	I9		
3615	B3			4177	I9		
3619	H9			4178	I9		
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3619	H9			4212	I9		
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3602	E6			4215	I9		
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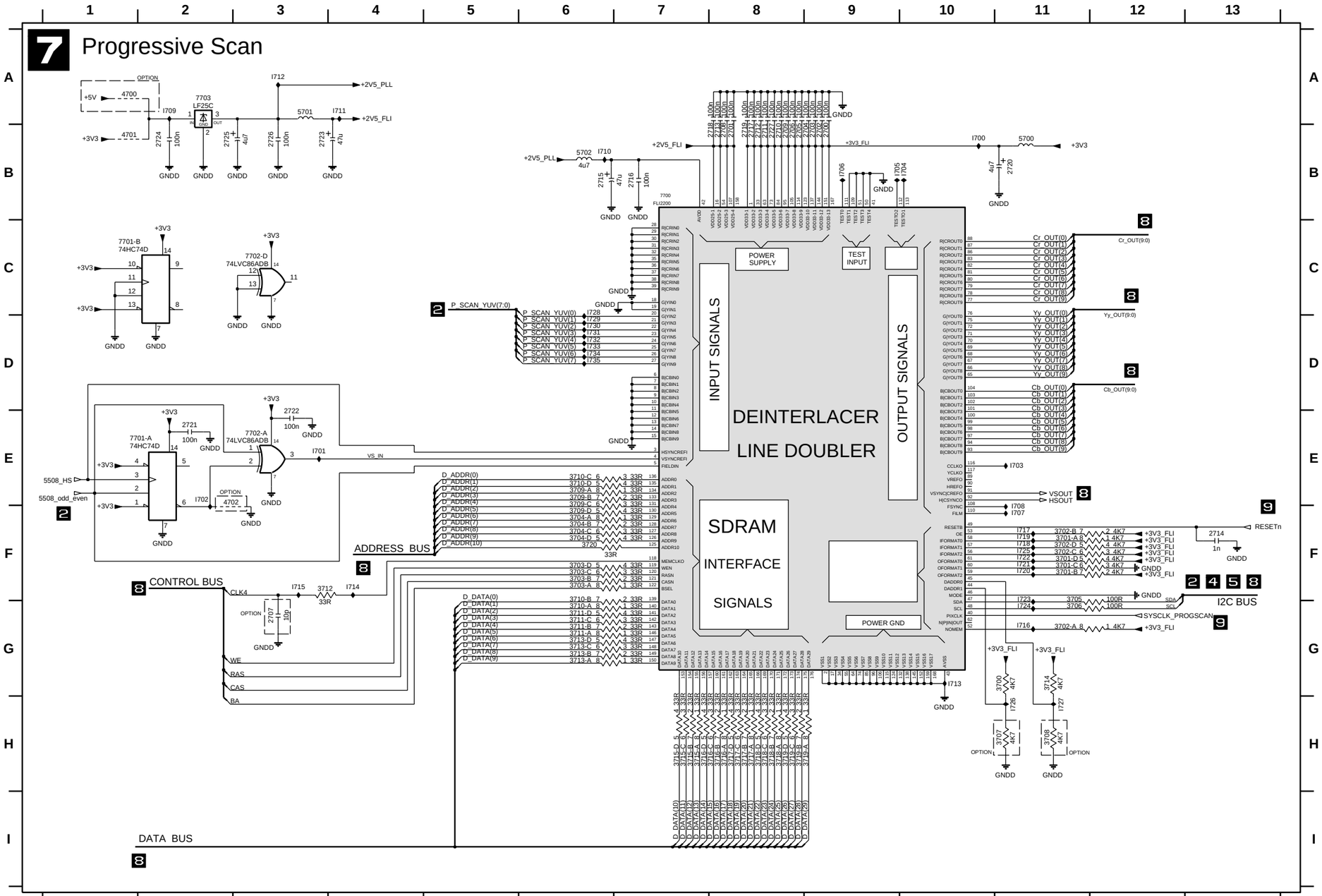
3610	C10			4223	I9		
3611	G5			4224	I9		
3612	G6			4225	I9		
3613	H6			4226	I9		
3614	C9			4227	I9		
3615	B3			4

■ SCHEMATIC DIAGRAM

DIGITAL: PROGRESSIVE SCAN



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2701	B8	3719-B	H8				
2702	B9	3719-C	H8				
2703	B9	3719-D	H8				
2704	B9	3720	F6				
2705	B8	4700	A1				
2706	B8	4701	B1				
2707	G3	4702	E2				
2708	B8	5700	B11				
2709	B8	5701	A3				
2710	B8	5702	B6				
2711	B8	7700	B7				
2712	B8	7701-A	E1				
2713	B8	7701-B	C1				
2714	F13	7702-A	E3				
2715	B6	7702-D	C3				
2716	B7	7703	A2				
2717	B8						
2718	B8						
2719	B8						
2720	B11						
2721	E2						
2722	E3						
2723	B3						
2724	B2						
2725	B2						
2726	B3						
2727	B8						
3700	G11						
3701-A	F11						
3701-B	F11						
3701-C	F11						
3701-D	F11						
3702-A	G11						
3702-B	F11						
3702-C	F11						
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3703-B	F6						
3703-C	F6						
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3704-A	F6						
3704-B	F6						
3704-C	F6						
3704-D	F6						
3705	G11						
3706	G11						
3707	H11						
3708	H11						
3709-A	E6						
3709-B	E6						
3709-C	F6						
3709-D	F6						
3710-A	G6						
3710-B	G6						
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3713-B	G6						
3713-C	G6						
3713-D	G6						
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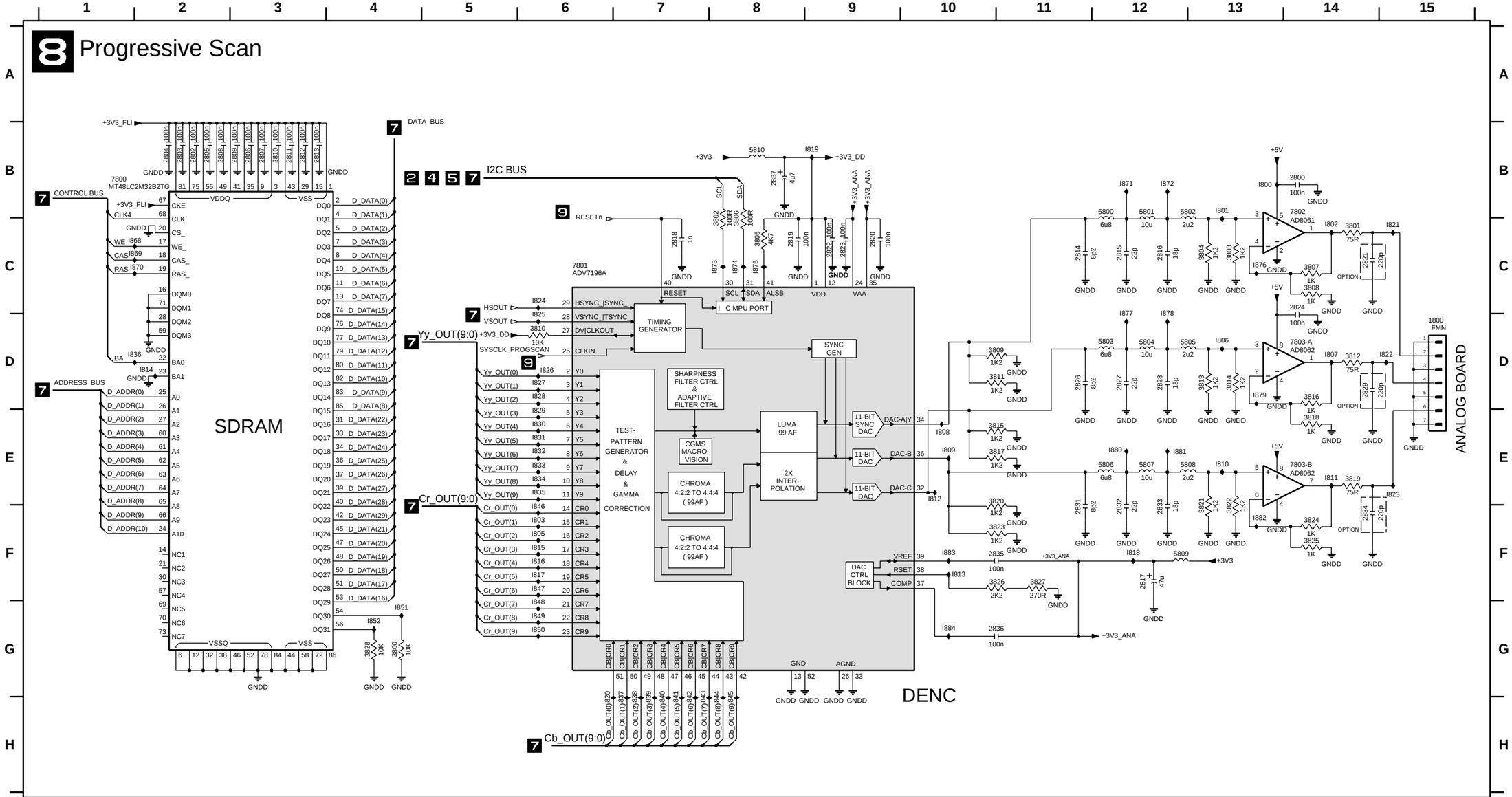
3715-B	H7						
3715-C	H7						
3715-D	H7						
3716-A	H8						
3716-B	H8						
3716-C	H8						
3716-D	H7						
3717-A	H8						
3717-B	H8						
3717-C	H8						
3717-D	H8						
3718-A	H8						
3718-B	H8						
3718-C	H8						
3718-D	H8						

■ SCHEMATIC DIAGRAM

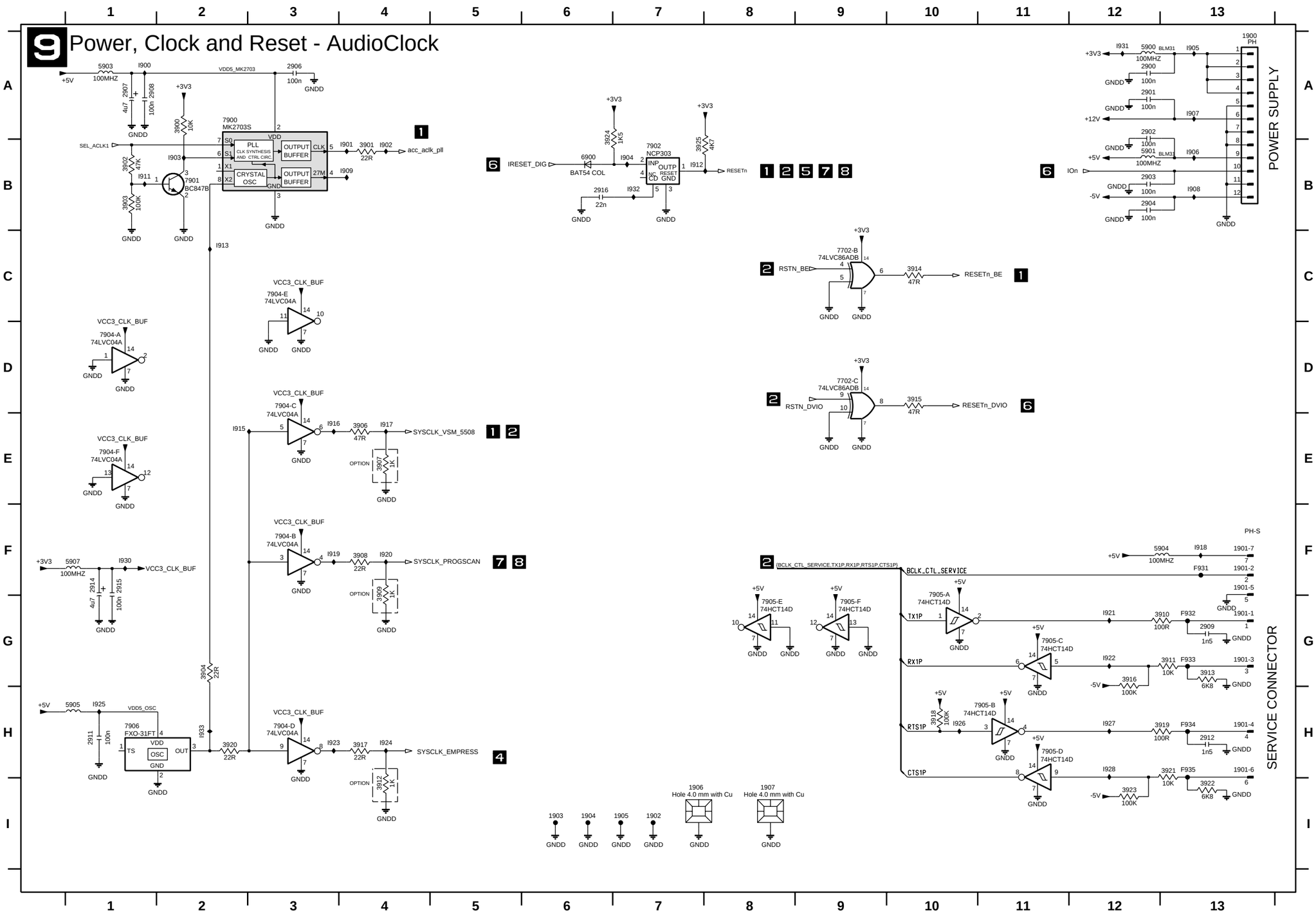
DIGITAL: PROGRESSIVE SCAN

1800	D15	2806	B3	2812	B3	2818	C7	2824	C14	2832	E12	3800	G4	3806	B8	3812	D14	3818	E14	3824	F14	5801	B12	5807	E12	7802	B14
2800	B14	2807	B3	2813	B3	2819	C8	2826	D11	2833	E12	3801	C14	3807	C14	3813	D13	3819	E14	3825	F14	5802	B12	5808	E12	7803-A	D14
2802	B2	2808	B2	2814	C11	2820	C9	2827	D12	2834	F14	3802	B8	3808	C14	3814	D13	3820	E10	3826	F11	5803	D12	5809	F12	7803-B	E14
2803	B2	2809	B3	2815	C12	2821	C14	2828	D12	2835	F10	3803	C13	3809	D10	3815	E10	3821	E13	3827	F11	5804	D12	5810	B8		
2804	B2	2810	B3	2816	C12	2822	C9	2829	D14	2836	G10	3804	C13	3810	D6	3816	D14	3822	E13	3828	G4	5805	D12	7800	B1		
2805	B2	2811	B3	2817	F12	2823	C9	2831	E11	2837	B8	3805	C8	3811	D11	3817	E11	3823	F11	5800	B12	5806	E12	7801	C6		



■ SCHEMATIC DIAGRAM

DIGITAL: POWER, CLOCK, AND RESET AUDIO CLOCK



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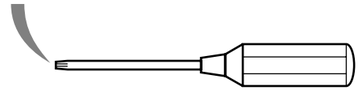
1901-2	F13
1901-3	G13
1901-4	H13
1901-5	F13
1901-6	H13
1901-7	F13
1902	I7
1903	I6
1904	I6
1905	I7
1906	I7
1907	I8
2900	A12
2901	A12
2902	A12
2903	B12
2904	B12
2906	A3
2907	A1
2908	A1
2909	G13
2911	H1
2912	H13
2914	F1
2915	F1
2916	B6
3900	A2
3901	B4
3902	B1
3903	B1
3904	G2
3906	E4
3907	E4
3908	F4
3909	F4
3910	G13
3911	G13
3912	I4
3913	G13
3914	C10
3915	D10
3916	G12
3917	H4
3918	H10
3919	H13
3920	H2
3921	H13
3922	I13
3923	I12
3924	A6
3925	B7
5900	A12
5901	B12
5903	A1
5904	F13
5905	H1
5907	F1
6900	B6
7702-B	C9
7702-C	D9
7900	A2
7901	B2
7902	B7
7904-A	D1
7904-B	F3
7904-C	D3
7904-D	H3
7904-E	C3
7904-F	E1
7905-A	G10
7905-B	H10
7905-C	G11
7905-D	H11
7905-E	G8
7905-F	G9
7906	H1
F931	F13
F932	G13
F933	G13
F934	H13
F935	H13

■ EXPLODED VIEW

U model

When disassembling, use the special screw driver with tip shape in figure.

T10	2.7 mm	for screws 21, 34 and 35
T8	2.2 mm	for screws 32
T6	1.7 mm	for screws 22, 31 and 33



DVDR LOADER

DVIO

DIGITAL

FRONT ASS'Y

ANALOG

P.S.U.

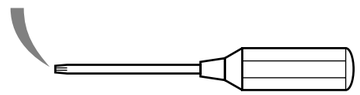
6	171 ~ 179	for Top Cover
6	204 ~ 210 215 217 218 255 ~ 258 284 ~ 286	for P.C.B. and Rear Panel
8	75 ~ 78	for Front Panel
10	192 ~ 195 271 ~ 277 279	for plastic parts
15	200 ~ 203	for DVDR Loader

■ EXPLODED VIEW

A, B, G model

When disassembling, use the special screw driver with tip shape in figure.

T10	2.7 mm	for screws 21, 34 and 35
T8	2.2 mm	for screws 32
T6	1.7 mm	for screws 22, 31 and 33



DVDR LOADER

DVIO

DIGITAL

FRONT ASS'Y

ANALOG

P.S.U.

6	171 ~ 179 for Top Cover
6	204 ~ 210 215 217 218 255 ~ 258 284 ~ 286 for P.C.B. and Rear Panel
8	75 ~ 78 for Front Panel
10	192 ~ 195 271 ~ 274 276 277 for plastic parts
15	200 ~ 203 for DVDR Loader

■ MECHANICAL PARTS

■ WARNING

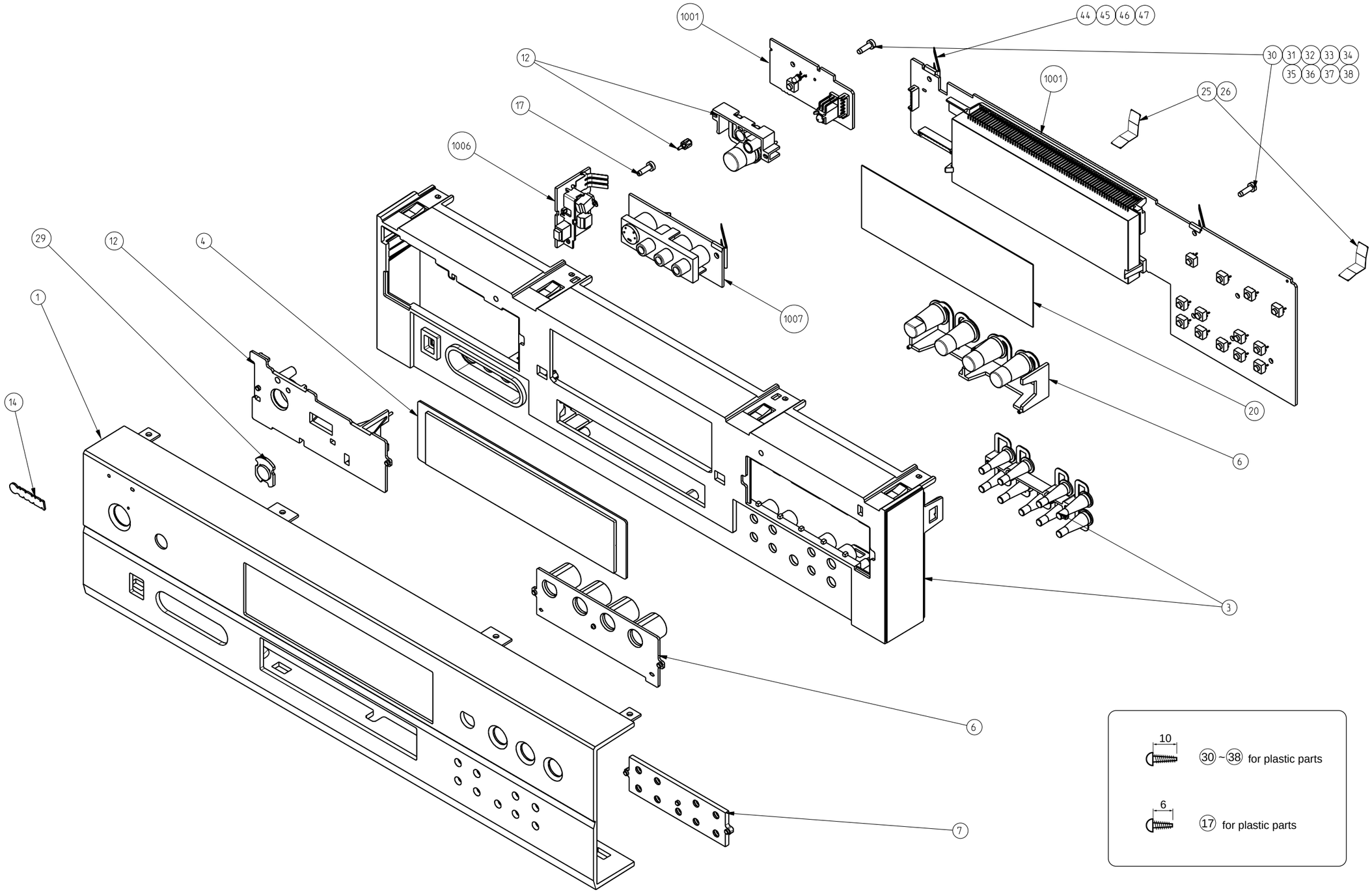
Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.

	Ref. No.	PART NO.	Description		Remarks	Markets
*	65	AAX44090	TRAY LID		3104 127 13741	U
*	65	AAX44120	TRAY LID		3104 127 13841	A
*	65	AAX44110	TRAY LID		3104 127 13821	B
*	65	AAX44100	TRAY LID		3104 127 13803	G
	75		SCREW 3MX8 WITH SPIKES	3x8	3104 120 40141	
	76		SCREW 3MX8 WITH SPIKES	3x8	3104 120 40141	
	77		SCREW 3MX8 WITH SPIKES	3x8	3104 120 40141	
	78		SCREW 3MX8 WITH SPIKES	3x8	3104 120 40141	
	81		BASIC ENGINE	VAE 8015	9305 025 81502	U
	81		BASIC ENGINE	VAE 8015	9305 025 81501	ABG
	151		COVER ASS'Y		3104 127 13852	
	152		SADDLE EDGE DS12SP KITAGAWA		8204 056 65311	
	153		EARTH SPRING		3104 122 00743	
	154		EARTH SPRING		3104 122 00743	
	155		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	156		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	171		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	172		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	173		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	174		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	175		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	176		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	177		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	178		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	179		SCR WASH TORX TAP ST ZN	3x6	3139 110 40611	
	181		FRAME		3104 121 24507	
	183		SPACER LOCKING CARD NY 9.8 B		2422 015 16118	
	184		SPACER LOCKING CARD NY 9.8 B		2422 015 16118	
	185		SPACER LOCKING CARD NY 9,8MM		2422 015 19499	
	186		SPACER LOCKING CARD NY 9,8MM		2422 015 19499	
	187		SPACER LOCKING CARD NY 9,8MM		2422 015 19499	
	188		SPACER LOCKING CARD NY 9,8MM		2422 015 19499	
	191		FILTER AIR INLED BOTTOM		3104 124 07455	
	192		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	193		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	194		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	195		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	196		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	197		DUST FILTER		3104 123 30002	
	198		FILTER AIR INLET COVER		3104 124 07733	
	199		DC BRUSHLESS FAN		3104 128 93031	
	200		SCR PAN TORX TAP ST ZN BK	3x15	2511 077 00046	
	201		SCR PAN TORX TAP ST ZN BK	3x15	2511 077 00046	
	202		SCR PAN TORX TAP ST ZN BK	3x15	2511 077 00046	
	203		SCR PAN TORX TAP ST ZN BK	3x15	2511 077 00046	
	204		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	205		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	206		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	207		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	208		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	209		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	210		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	211		SPACER CARD NY NT 19.2MM B		2422 015 19553	
	212		SPACER CARD SHIELDED		8204 056 07961	
	213		SADDLE MINI CLAMP TYPE B11.8		2422 015 16901	
	214		SADDLE WIRE NY6/6 23.7MM B		2422 015 17636	
	215		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	217		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	218		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	251		FOOT SILVER ASS'Y		3104 127 10742	
	252		FOOT SILVER ASS'Y		3104 127 10742	
	253		FOOT SILVER ASS'Y		3104 127 10742	
	254		FOOT SILVER ASS'Y		3104 127 10742	
	255		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	256		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	257		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	258		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	266		BACKPLATE ASS'Y		3104 127 14751	U
	266		BACKPLATE ASS'Y		3104 127 14741	ABG
	268		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	270		EARTH SPRING TUNER		3104 121 24472	
	271		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	272		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	273		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	274		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	277		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	278		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	280		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	281		SCR PAN TORX TAP ST ZN BK	3x8	2511 076 50012	
	284		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	285		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
	286		SCR PAN TORX TAP ST ZN BK	3x6	2511 077 00039	
⚠	1002		PSU DVDR1000-2 EURO 50PS203		3122 427 22713	
⚠	1003		DVDR ANAL.BOARD E1.5 DSM		3103 608 50362	
⚠	1005		NEC DV-BOARD VIENNA		3103 608 50265	
	8001		CWAS FLEX DVD 22 70 32S		3104 157 11641	
	8002		CWAS FLEX DVD 22 70 32S		3104 157 11641	
	8004		CWAS FLEX DVD 10 110 32S		3104 157 11531	
	8006		CWAS 04EH/04PH 350 2X2		3104 157 11601	
	8007		CWAS 7EH/7EH 360 26S		3104 157 11552	
	8008		CWAS 8EH/8PH 280 26S		3104 157 11562	
	8011		CWAS 12EH/12PH 420 6+6 26S		3104 157 12172	
	8013		CABLE IEEE-1394 4P AMP		3104 128 92921	

* New Parts

* New Parts

■ EXPLODED VIEW (FRONT ASS'Y)



■ MECHANICAL PARTS (Front Ass'y)

	Ref. No.	PART NO.	Description		Remarks	Markets
			FRONT-ASS'Y-COMPLETE			
*	1	AAX44140	FRONT PANEL		3104 127 13666	
*	3	AAX44060	SUBPANEL ASS'Y		3104 127 13674	
*	4	AAX44040	WINDOW		3104 127 14343	
*	6	AAX44160	HOLDER RIGHT ASS'Y		3104 127 13702	
*	7	AAX44150	PLATE RIGHT		3104 124 08333	
*	12	AAX44170	HOLDER LEFT ASS'Y		3104 127 13722	
*	14	AAX44050	EMBLEM		3104 120 00432	
	17		SCR PAN TORX TAP ST ZN BK	3x6	2511 076 50011	
	20		FILTER		3104 124 08862	
	25		EARTH SPRING		3104 121 24874	
	26		EARTH SPRING		3104 121 24874	
*	29	AAX43990	IR WINDOW		3104 124 08855	
	30		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	31		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	32		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	33		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	34		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	35		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	36		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	37		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	38		SCR PAN TORX TAP ST ZN BK	3x10	2511 076 50013	
	44		EARTH SPRING		3104 121 22514	
	45		EARTH SPRING		3104 121 22514	
	46		EARTH SPRING		3104 121 22514	
	47		EARTH SPRING		3104 121 22514	
	351		LABEL		3103 176 02991	
	352		FOIL THERMO TRANSFER		3103 103 26591	
*	1001	AAX44000	P.C.B. ASS'Y	DISPLAY, IR & STANDBY	3104 128 08513	
	1006		PCB ASSY 4319 DVIO-FRONT	FRONT DV INPUT	3104 128 07611	
	1007		FC-BOARD	FRONT AV INPUT	3103 608 50231	
	8005		CWAS 09PH/09PH 420 3X3 SH		3104 157 11631	
	8009		CWAS 12PH/12PH 340 6+6 BK		3104 157 02042	

* New Parts

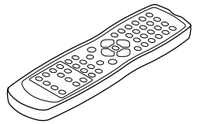
■ MECHANICAL PARTS (Accessories)

■ **WARNING**
Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equal to those originally installed.

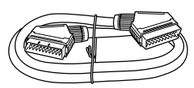
	Ref. No.	PART NO.	Description		Remarks	Markets
			ACCESSORIES			
*	300	AAX44180	REMOTE CONTROL		3139 238 02431	
*	302	AAX44070	SCART CABLE	1.5m	3104 128 90582	ABG
*	303	AAX44030	S-VIDEO CABLE	1.5m	3104 128 93041	
*	304	AAX44080	AUDIO PIN CABLE, GOLD PLATED	2P 1.5m RE/WH	3104 157 11022	
*	305	AAX44130	VIDEO PIN CABLE, GOLD PLATED	1P 1.5m YE	3104 128 92491	
*	306	AAX44190	AUDIO/VIDEO CABLE, GOLD PLAT	3P 1.5m GR/BE/RE	3104 128 92771	U
*	307	AAX44010	RF CABLE	1.5m	3104 128 90403	U
*	307	AAX44020	RF CABLE	1.5m	3111 170 21592	ABG
* ⚠	308	AAX44200	POWER CABLE	1.8m	3104 128 92561	U
* ⚠	308	AAX44230	POWER CABLE	1.8m	8222 641 42821	A
* ⚠	308	AAX44210	POWER CABLE	1.8m	4622 001 60591	B
* ⚠	308	AAX44220	POWER CABLE	1.8m	4622 004 50291	G
*	309	AAX43980	DVD+RW DISC	4.7GB	9082 100 01504	
			BATTERY		9299 000 84913	

* New Parts

300



302



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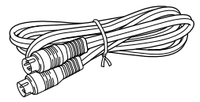

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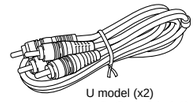
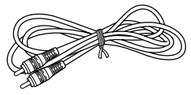


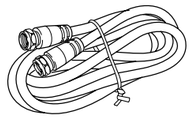
U model (x2)
A, B, G models (x1)

305

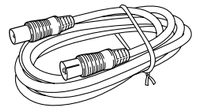


306

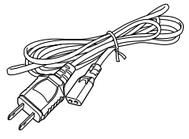
307(U model)



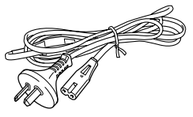
307(A,B,G models)



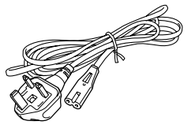
308(U model)



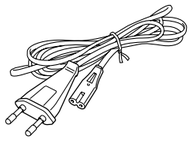
308(A model)



308(B model)



308(G model)



309

DRX-1

YAMAHA